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RESEARCH AND DEVELOPMENT OF MULTI-MOTOR AC PROPULSION SYSTEMS

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Prepared for the

Transport Canada
Research and Development Centre

by

Department of Electrical Engineering
University of Toronto

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"The contents of this report reflect the views of the contractor and not necessarily the official views or policies of the Transport Canada Research and Development Centre."

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17. Abstract

This report concludes a research program undertaken for the development of an AC propulsion system. Steady-state and dynamic tests on a test set-up with two 150 hp AC squirrel cage motors were performed in order to consolidate the research findings of two previous reports (see item 15). In this final report, the objectives and the details of the test results along with the basic design relationships useful in specifying component ratings are presented. The specifications, basic operation and detailed system descriptions of the units are provided in the corresponding appendices. The findings verify that the operation of a current source inverter supplied by a current source fixed frequency chopper is the preferred system for traction applications.

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17. Résumé

Ce rapport complète un programme de recherche sur la mise au point d'un mode de propulsion par moteur à courant alternatif (CA). On y trouve les résultats d'essais tant statiques que dynamiques faits sur un banc d'essais incluant deux moteurs, chacun d'une puissance de 150 c.v. et du type cage d'écureuil. Le tout servit également à consolider les résultats obtenus au cours de recherches antérieures. En plus d'une présentation détaillée des objectifs et des résultats, le rapport contient aussi les éléments de base pour le design et la spécification des différentes composantes. Les spécifications, le mode d'opération et la description détaillés du système sont inclus dans les annexes. On y établi également que le système préféré consiste en un onduleur de courant alimenté par un hacheur de courant à fréquence fixe.

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CHAPTER 1

INTRODUCTION

1. INTRODUCTION

The work described in this report is based on the [1,2] earlier reports, "Development of an AC Motor Propulsion System for Rail Applications", Report No. TP232 and "AC Motor Propulsion Systems for Multi-Axle Drives", Report No. TP1431. In these reports, the feasibility of using a squirrel cage induction motor (to replace the dc motor) in rail applications, for both single axle and multi-axle drives, has been demonstrated.

The earlier reports show that on the basis of ruggedness, reliability, weight, volume and cost considerations, the chopper current source inverter system is the "preferred" system for operating an ac induction motor in traction environment. In comparison with the voltage source pulse width modulated (P.W.M.) system, the current source system has the following advantages:

(1) To obtain fixed frequency harmonics (communication, noise, resonance, etc.) in the input lines, P.W.M. voltage source system requires a two quadrant chopper and a second filter network. The resulting system is larger in the number of components, complexity, weight, losses, etc. in comparison with a current source system.

(2) All types of control strategies (slip frequency, power factor, flux control) can be implemented with a current source inverter.

(3) Noise and size of the current source inverter system can be reduced by using transistors in the input chopper current source.

The report [2] on the multi-axle ac drives has developed the analysis and design techniques for evaluating the various possible current source inverter configurations for multi-axle/multi-motor applications. This report shows that for the multi-axle applications, (e.g. Toronto T.T.C.)

where a significant wheel diameter differential cannot be avoided (a wheel diameter differential above .2% is considered significant), the "preferred" configuration (option D) basically consists of:

(1) A common chopper current source.

(2) A separate current source inverter for each motor with individual frequency control employing power factor or slip frequency regulation.

Figure 1.1 shows the block diagram of the "preferred" configuration of a multi-axle ac traction drive system with the inverters connected in parallel. The power circuit of this drive system is constituted of:

(a) Input filter, L_{if}-C_{if}: This filter limits the injection of current harmonics, due to the chopper operation, back into the dc power supply. The determination of L_{if} and C_{if} depends on the chopper rating, chopper frequency and to a large extent on the harmonic restrictions imposed by the power supply.

(b) Chopper protective inductance, L_{ℓ}: This inductance limits the rate of rise of the current in the chopper main thyristors. The size of inductance L_{ℓ} depends on the maximum allowable current rate of rise of the selected main thyristors and on the chopper input voltage, V_{ic}.

(c) 2-quadrant chopper current source: This unit supplies the inverters with the required dc input currents. The power and logic circuits of this chopper are fully detailed in Appendix C. This chopper operates under a constant chopping frequency and is capable of regeneration. The advantages of using this type of chopper instead of the one with an earlier design in the traction applications are outlined later in this chapter.

(d) dc link current filter inductors, L_{f1}, L_{f2}: These inductors filter out the high frequency components of the chopper output voltage to provide smooth dc currents. They also serve to maintain constant dc input currents during current switchings in the inverters. The design of L_{f1} and L_{f2}

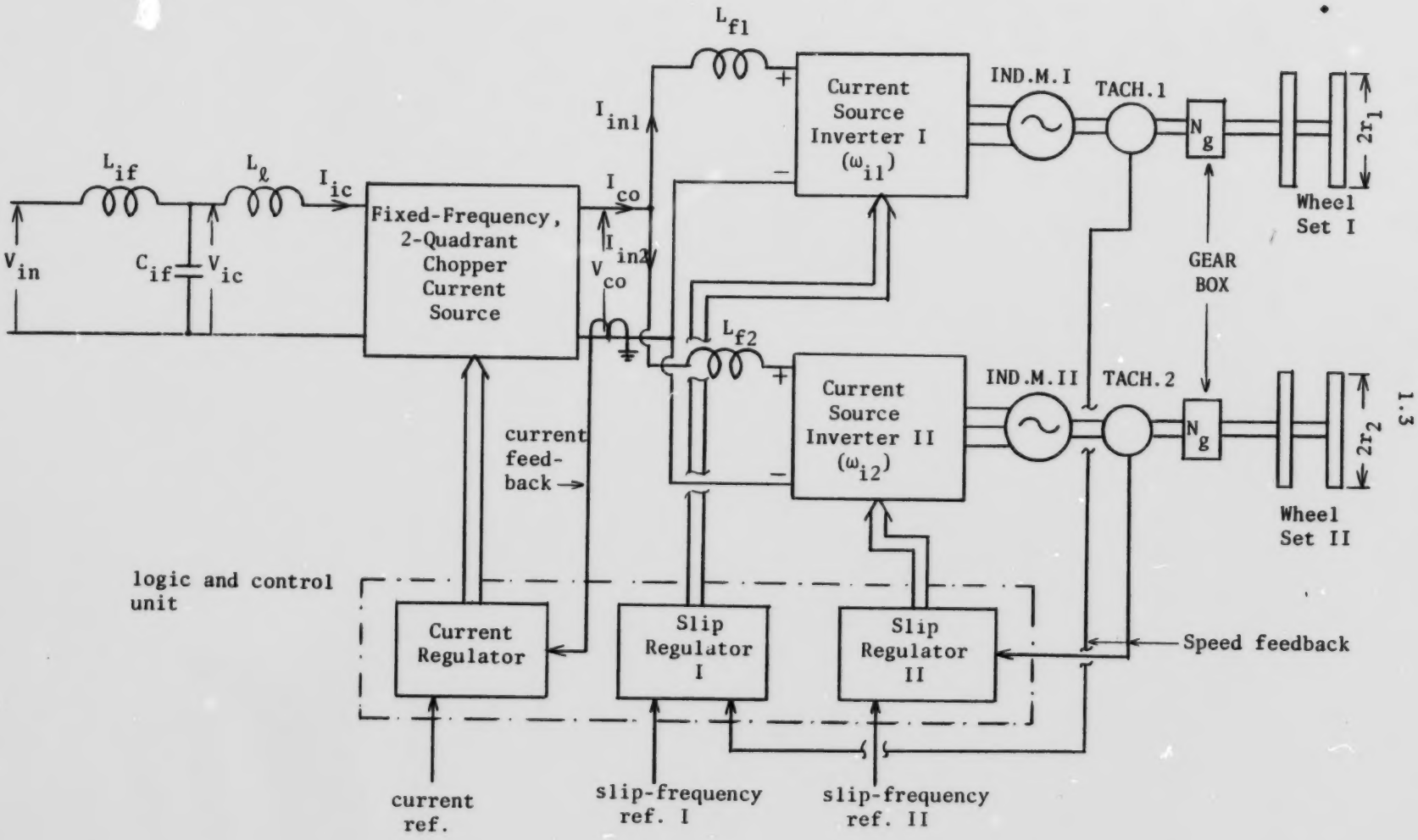


Fig. 1.1 Block diagram of the 'preferred' configuration of a multi-axle traction ac drive system with the inverters connected in parallel.

depends on the accepted rms value of the ripple current (in per centage of the dc link average current).

(e) Current source inverters: The design of the two current source inverters is quite similar to each other. Each inverter is of the sequentially commutated current source type. A detailed description of the power and logic circuits for this type of inverter is given in Appendix D. Generally, the output frequencies of the inverters are not the same. Each inverter is capable of operating in four quadrants. However, in this application only the operations in the 1st and 4th quadrants are considered.

(f) Squirrel-cage induction machines: The required power for moving a vehicle is supplied by the induction machine mounted on each axle. The selection of these machines depends on the torque and power profiles of the vehicle versus its speed. Each wheel set receives its torque from the corresponding machine through a gear box with a reduction ratio of N_g. The value of N_g depends on the motor and vehicle top speeds and also on the wheel set radius.

The chosen control strategy is the slip frequency control. The elements of this type of control as depicted in Figure 1.1 are:

(a) Tachometers I and II: A digital tachometer on the shaft of each drive motor provides signals proportional to each motor shaft speed. The speed feedback signals from each tachometer constitute an input to the corresponding slip frequency regulator.

(b) Slip frequency regulators I and II: Each regulator in Figure 1.1 adjusts the output frequency of the corresponding inverter such that, at the required motor speed, the established slip frequency becomes the same as the slip frequency reference. Depending on, the motoring/braking mode of operation, the operation in the constant torque/power region and the

series/parallel connection of the inverters, the slip frequency reference for the two inverters might be different.

(c) Current regulator: The generated thrust by each wheel set depends on the magnitude of the chopper output current. The current regulator adjusts the required chopper output current according to the input requirement (current reference).

The lower power (5 HP) feasibility of both single and multi-axle current source inverter systems has been demonstrated in the earlier contracts [1,2]. The basic objective accomplished in this contract is the feasibility of operation of similar but higher power systems. To achieve the above the following have been done:

(1) Constructing the breadboard modules to perform tests outlined in 2, 3 and 4 at about 250 kilowatt level and prove the feasibility of the design with a typical traction load.

(2) Performing complete steady-state tests (for a single motor set-up) at various operating points of the typical traction torque speed curve at nominal 600 volt dc input and 125 HP at the break point. The relevant quantities measured were component ratings, harmonics currents and voltages, systems power flow, losses in the system elements, etc. The tests were performed in both the motoring and the braking regions.

(3) Executing system dynamic tests to identify functional problems and establish the capability of determining the system frequency response such that the propulsion systems can be simulated with a vehicle model. The capability of the electrical simulation of the desired torque-speed profile enables the test modules to simulate any general vehicle performance specification.

(4) Performing tests outlined in 2 on two motor system using one chopper and two current source inverters (the option D system established in reference 2).

The above objectives have been achieved by designing and building six converter modules such that all the units, while all the necessary test results are obtained, can operate continuously under rated conditions. The six units (Figure 1.2) needed and their major functions are:

(1) DC Power Supply Unit: Contains a controlled rectifier (P) and filter to deliver 600-volt dc from 460-volt ac line and a line commutated inverter controlled rectifier (N) to clamp the dc back to ac line. The ac power to the controlled rectifier P and N is supplied from isolated windings on the input transformer.

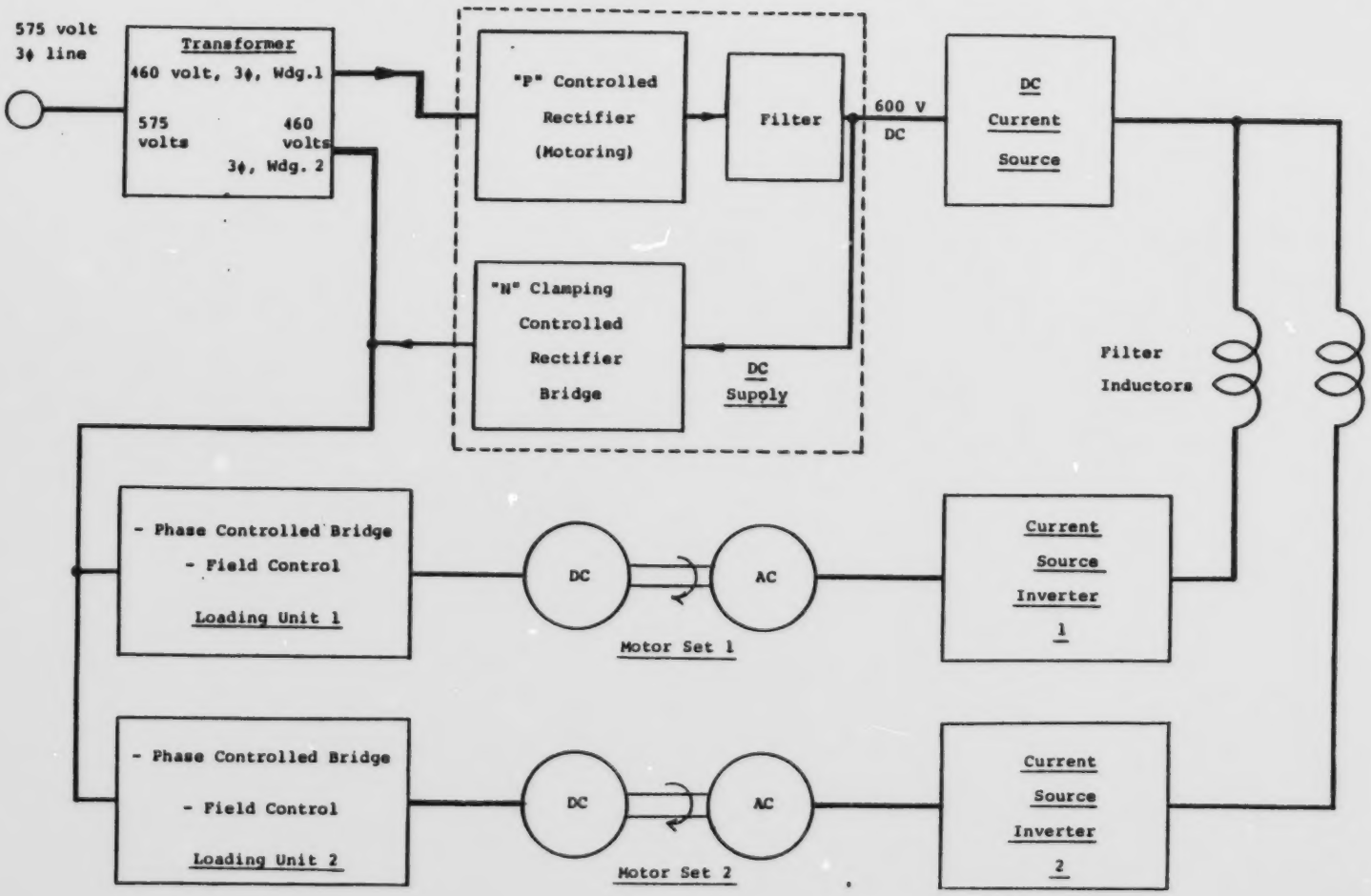
(2) Chopper Current Source Unit: Provides the current source for the inverters from the 600-volt bus and can operate in both motoring and braking regions.

(3) Current Source Inverter Unit 1: Supplies three-phase ac current to motor set 1 and can operate in four quadrants.

(4) Current Source Inverter Unit 2: Supplies three-phase ac current to motor set 2 and can operate in four quadrants.

(5) Loading Unit 1: Supplies armature and field for motor set 1 from ac line and can operate in four quadrants.

(6) Loading Unit 2: Supplies armature and field for motor set 2 from ac line and can operate in four quadrants.



FIG,1.2- BLOCK DIAGRAM OF THE TWO-MOTOR SYSTEM

Design Features of Units

Some of the significant design features of the units (dc power supply unit, loading unit, chopper current source unit and current source inverter unit) are given in the following. The details of the circuit and the operation of these units are presented in Appendices A, B, C and D respectively.

(1) All the units are packaged units with good accessibility to provide ease of monitoring (or measuring) waveforms both in the power and logic circuits. The logic and control circuits are printed circuit boards wherever possible. Also Augat boards with flexible firm plug-in leads are used where circuit modifications must be made to achieve the required modes of operation.

(2) The instrumentation requirements for power loss measurements in the inverter and the current source units require a precision which is practically not possible with any instrumentation technique except water cooling. Therefore, the inverter and current source units employ water cooling and means have been provided to measure water flow and both inlet and outlet water temperatures.

(3) A great deal of effort has been spent in planning the details of the instrumentation. Meters have been provided to display voltage, current, power, etc. (inside the power units) for steady state display within ±2% full scale accuracy. All the key system quantities needed during the tests are available in <u>isolated</u> analog form such that the signals can be recorded on a tape and processed on the main University of Toronto computer. This instrumentation system ensures ±5% accuracy and should be adequate for the dynamic tests. All the key waveforms (steady-state voltages and currents) which need detailed processing

(harmonic components, etc.) can be stored on a 16 k memory by direct analog to digital conversion. The stored data can be transferred to a magnetic tape using 6800 microprocessor development system. The data on the magnetic tape can be processed on the main University of Toronto computer.

(4) The interconnection of the system modules (power supply, chopper, inverter and loading units) has been arranged with plug-in connections and module units. The power supply transformer has been enclosed in a fence and an automatic contactor arrangement has been installed to limit the inrush current. A waterflow switch with an alaram has been incorporated to ensure that the transformer is not destroyed with any interruption of the water flow. Three fuse disconnects have been installed on the wall, two for the power supply unit and the third for the loading unit. All the power interconnections are made such that no high voltage power connections are bare.

The major change in the design of the system respect to the earlier configuration has been occurred in the chopper current source, Figure 1.3. In the new scheme, Figure 1.4, the chopper output and as a result the inverter(s) input current(s) are controlled by pulse width modulation technique. In this strategy of controlling the chopper output, a fixed chopping frequency is applied to the chopper current source. The advantages of such a control strategy are:

(a) The input current of the chopper contains harmonics of the chopping frequency. Therefore, by choosing a high chopping frequency (800 Hz to 2 KHz), the size of the input filter can be reduced.

(b) A fixed chopping frequency simplifies the elimination of interference with the signalling and commutation frequencies.

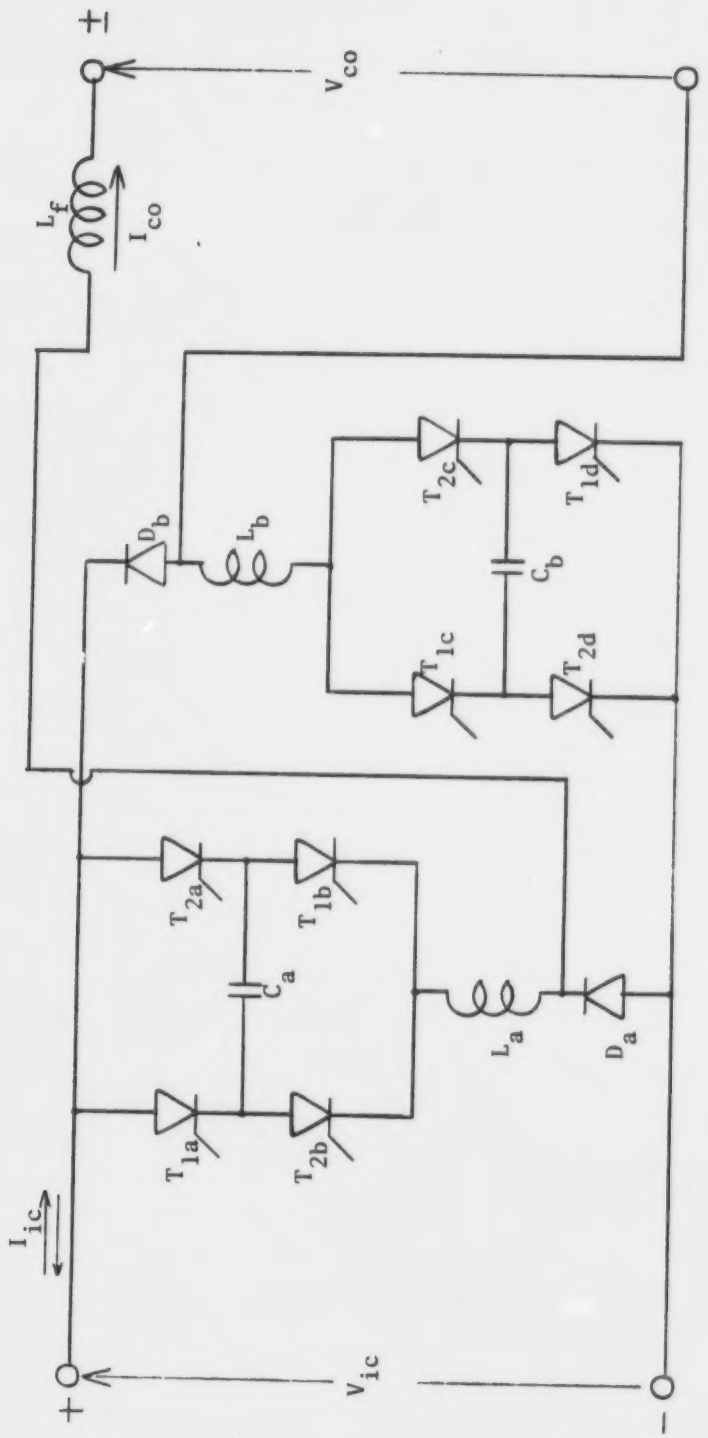


Fig. 1.3 Power circuit configuration of the variable frequency, 2-quadrant chopper current source used in an earlier design.

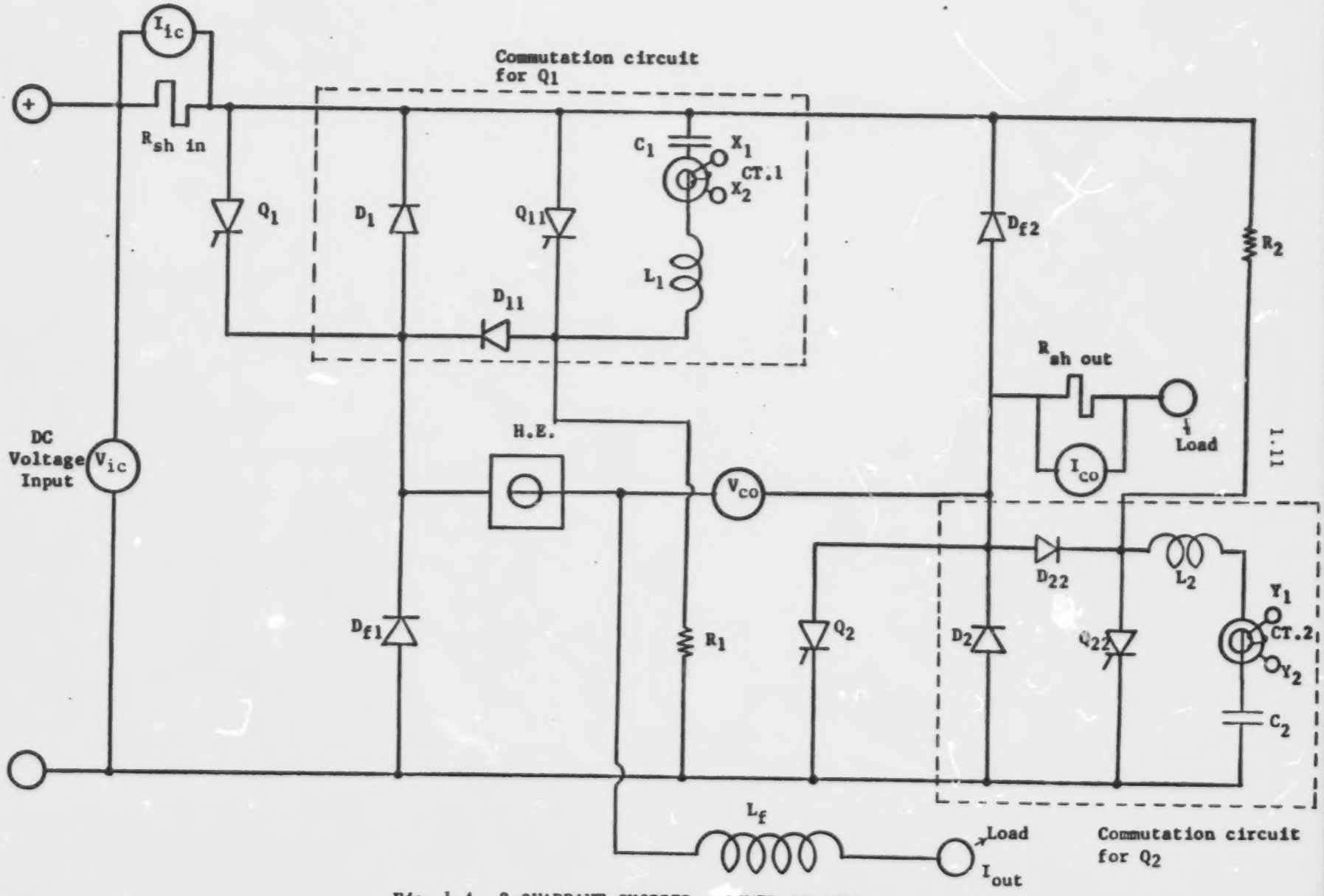


Fig. 1.4 2-QUADRANT CHOPPER - POWER CIRCUIT

(c) The maximum output (input) ripple voltage (current) in a fixed-frequency control strategy is one half of the corresponding value in a variable chopping frequency control (frequency modulation).

(d) It is possible to decrease the chopper output voltage to zero without altering the chopping frequency. (This technique could eliminate the humming noise in the Toronto Subway Cars.)

In addition, with the incorporated protection schemes, the chopper unit is quite rugged and reliable. As an example, the current-limit protection circuit monitors the instantaneous load current and commutates the load current if it exceeds the commutation capability of the circuit. In this way, the chopper is kept off until the load current becomes lower than the limit set by the protection circuit.

In the University of Toronto we have also implemented the microprocessor-based control in this type of chopper. References [117]-[119] in the Bibliography give detailed descriptions in this regard.

Figure 1.5 shows the mechanical loading set-up of a single-motor drive including the torque transducer, a 125 kilowatt separately excited dc machine and a 125 HP squirrel cage induction motor. This set-up provides continuous fast response readings of both torque and speed. Several problems were encountered in the mechanical alignment of the two motors and the torque transducer. The most serious problem was the mechanical resonance around 1000 rpm and this problem has been solved by realignment and a modified bearing. Figures 1.6 - 1.8 show respectively the details and specifications of the inverter, 2-quadrant chopper, dc power supply and dc loading, units.

The other sections of this report are as follows. Section 2 covers the objectives, test set-up and the test results of the experimental ac propulsion drive system. The design procedures for the current source inverter unit, chopper current source and selection of ac induction motor,

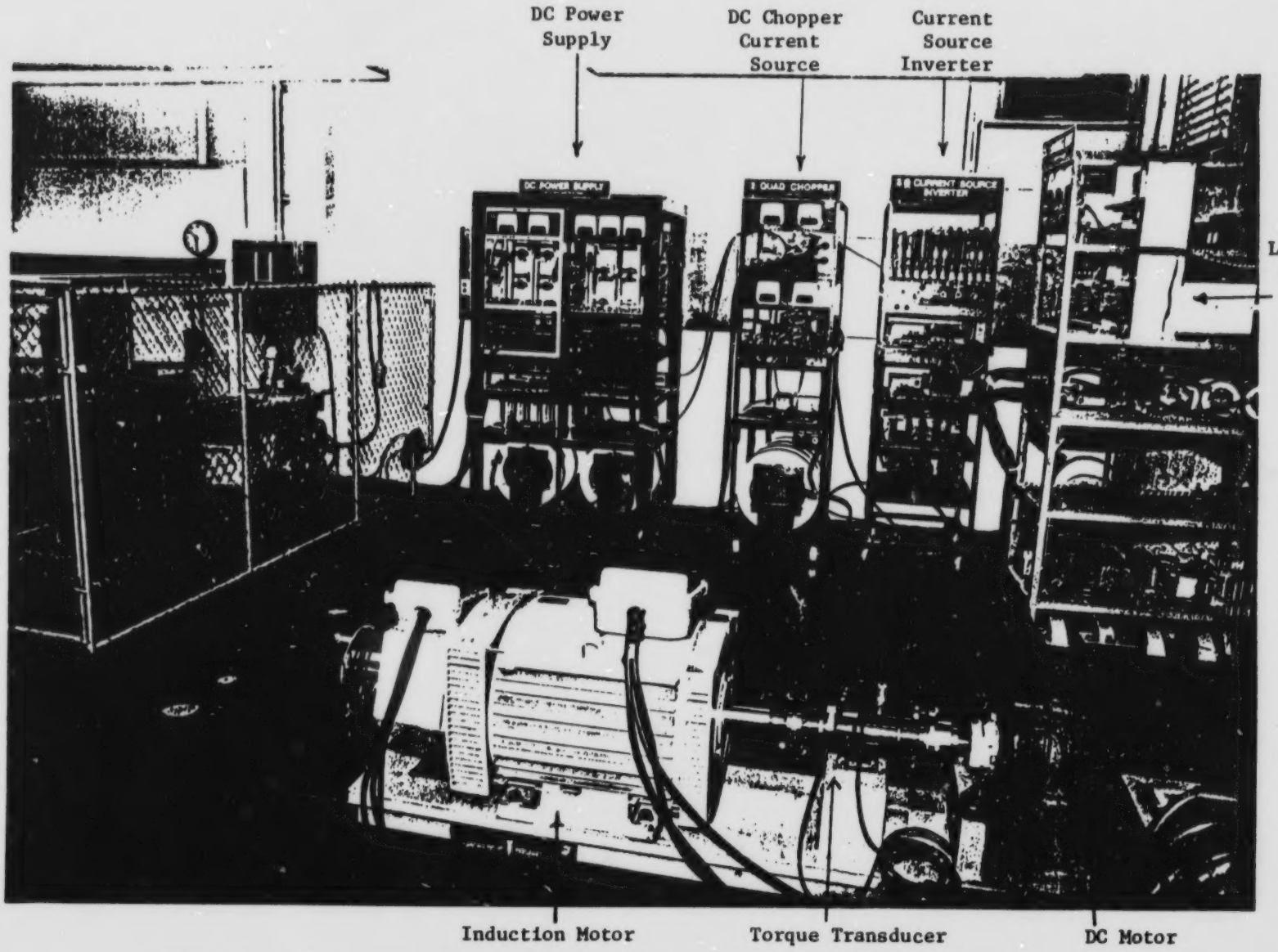


Figure 1.5 Photograph showing the interconnected modules for testing single motor ac propulsion system.

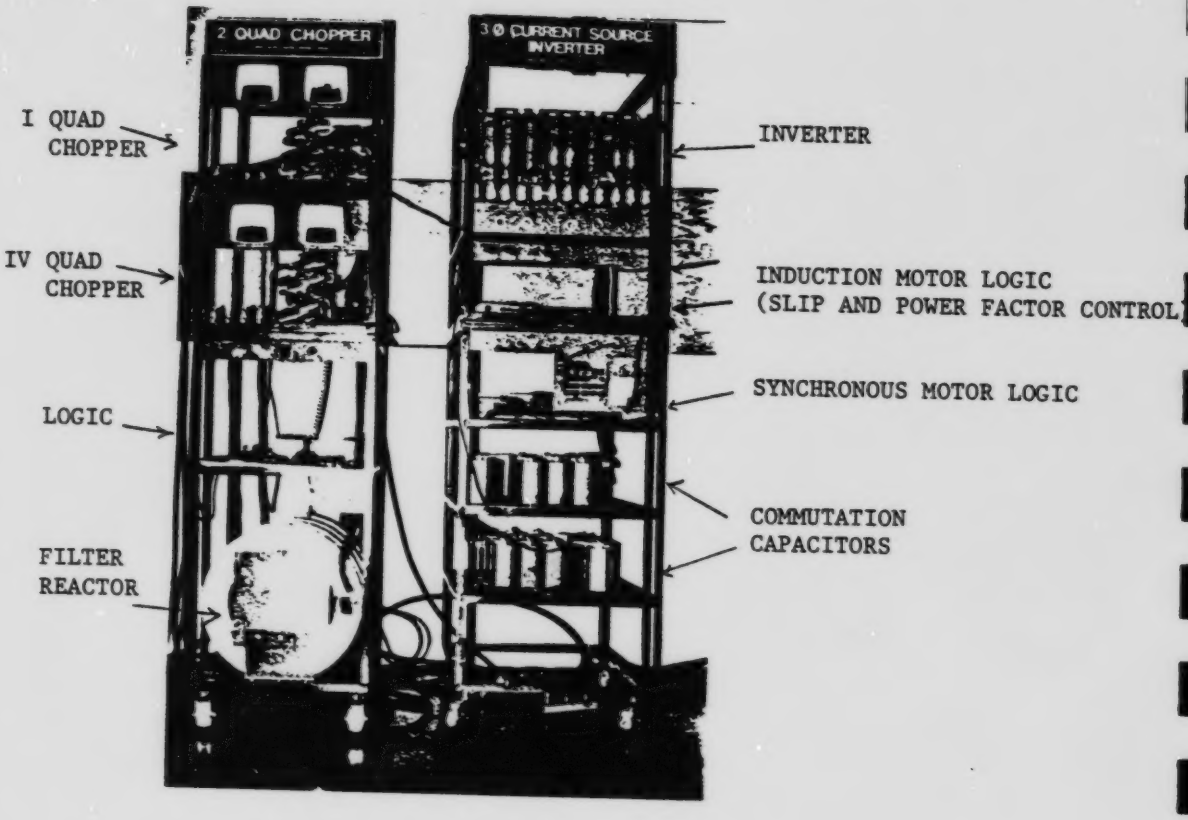


Fig. 1.6

PHOTOGRAPH SHOWING THE CHOPPER CURRENT SOURCE (2 QUAD CHOPPER) AND 3ϕ CURRENT SOURCE INVERTER UNITS

Chopper Current Source; 600 volt d.c. Input, Output ± 0 to 600 volt d.c., 400 Amperes.

Current Source Inverter supplied from the Chopper Current Source, Output 0 -500 volt a.c., 300 amps line current, 0 - 150 Hertz.

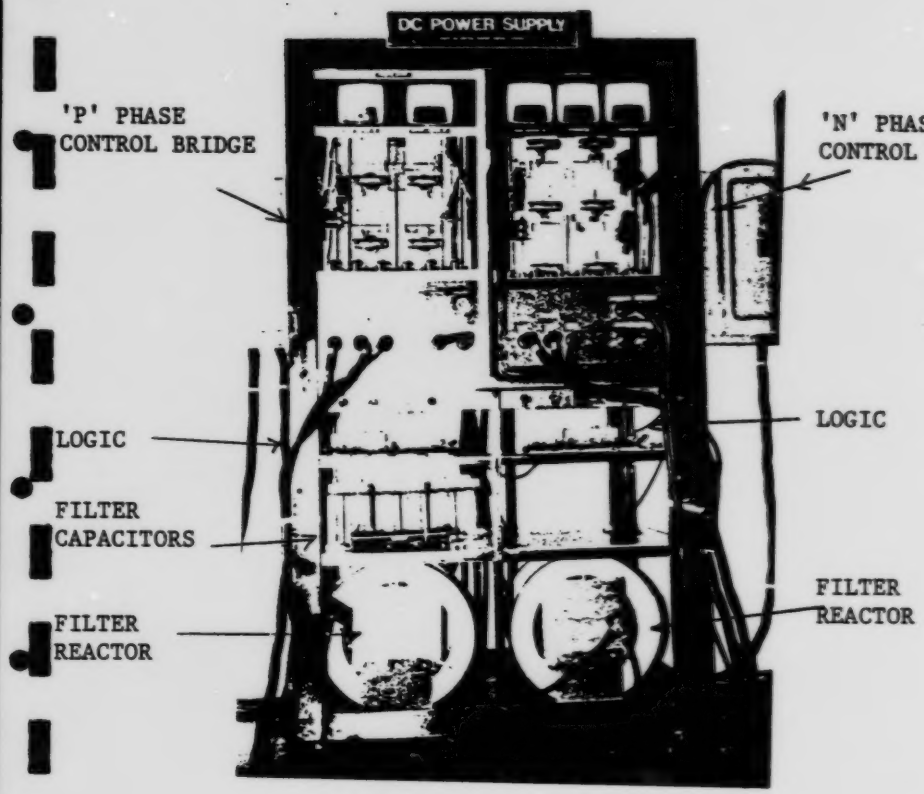


Fig. 1.7

PHOTOGRAPH SHOWING DETAILS OF DC POWER SUPPLY (3ϕ 460 VOLT INPUT, OUTPUT 0 - 600 VOLT DC, $\pm$ 400 AMPS).

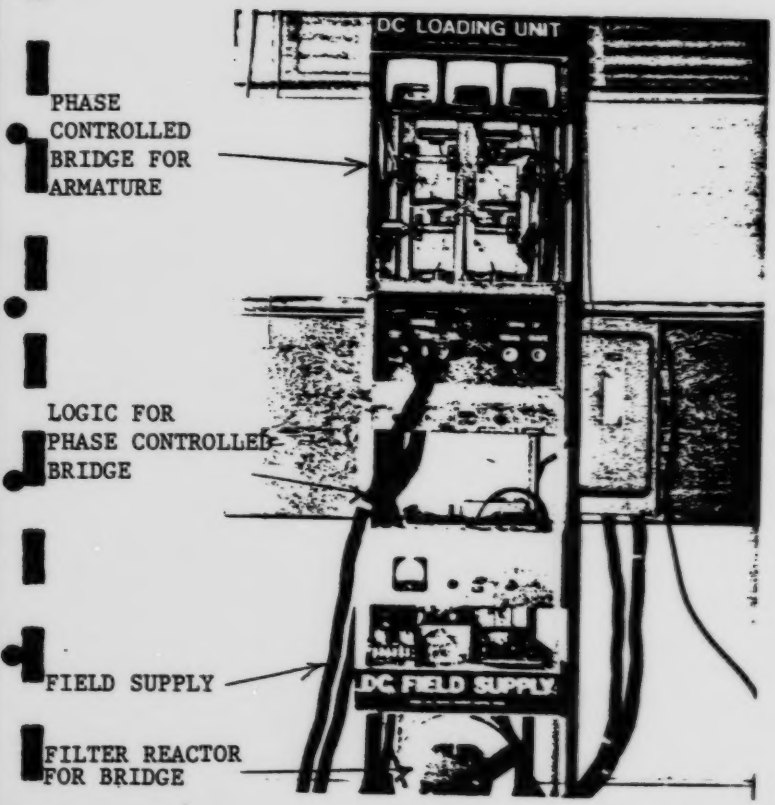


Fig. 1.8

PHOTOGRAPH SHOWING DETAILS OF DC LOADING UNIT

INPUT → 3ϕ, 460 VOLT, 60 HERTZ

OUTPUT FOR ARMATURE;

$\pm$ 0 - 600 VOLT DC, 200 AMPS

OUTPUT FOR FIELD

0 - 600 VOLT DC, 10 AMPS.

both for a single-axle and for a multi-axle drive system, are outlined in Section 3. Section 4 discusses the conclusions of this project following which the references and a comprehensive list of bibliography related to this project are included. Finally, the detailed descriptions of the operation of the power and logic circuits of the dc power supply, dc loading, chopper current source and current source inverter, units are provided in Appendices A, B, C and D, respectively.

CHAPTER 2

AC PROPULSION TESTS

2. AC PROPULSION TESTS

This chapter describes in detail the objectives, the requirements of the test modules and the steps involved in the performed tests of the current source inverter ac squirrel cage induction motor drives for one-motor and two-motor (multi-axle) applications. Four tables outline the details of the quantities measured on the, dc supply unit, chopper current source unit, current source inverter unit(s), and loading unit(s) all at various steady state operating points of a typical traction torque-speed curve. These results form the basics of design procedures established in Chapter 3.

2.1 Objectives

The major objectives of the tests have been the experimental verification of the design procedures outlined in earlier reports [1]-[2] and the demonstration of the feasibility of operation of units with higher power levels than those observed earlier. In addition, the results have been employed to modify the previous design relationships, wherever necessary, and establish the fundamental design procedure for each unit in a step-by-step method (Chapter 3). The execution of dynamic tests to identify functional problems and providing solutions; the examination of the effects of the harmonics in the input dc line on the input filter configuration and the selection of the motor voltage and slip frequency at the base speed, have also been among the principal objectives of the tests.

The detailed steps in the test program are outlined in section 2.3 and consist of both the steady-state and the dynamic tests. The steady-state tests were performed (for both single and two motors) at various operating points of the typical traction torque speed curve (Fig. 2.1) at nominal 600 volts dc input. The relevant quantities that were measured are component ratings, harmonic currents and voltages, system power flow, losses in the system elements, etc.

The major change in these tests compared with earlier ones has been in the modification of the chopper current source configuration and consequently in its control strategy from frequency modulation (variable chopping frequency) to pulse width modulation (fixed chopping frequency). The advantages of the new control scheme were outlined in Chapter 1.

The tests were performed in both the motoring and the braking regions. The dynamic tests were performed to identify functional problems and establish the capability of determining the transfer function of the ac propulsion system which can be employed to calculate the dynamic performance of a vehicle if a vehicle model and specifications [2] are available.

2.2 Test Set-Up

The block diagram of the test set-up for the two-motor system is shown in Fig. 2.2 and the details of the units are described in appendices A, B, C and D. A brief description of the requirements and the features of the units are discussed in this section.

The basic test set-up consists of a dc power supply unit, (a transformer, P and N 3-phase controlled rectifiers and a filter), a dc (chopper) current source, two filter inductors, two current source inverter units and two loading units (phase controlled bridge or controlled rectifier and a dc chopper for field control).

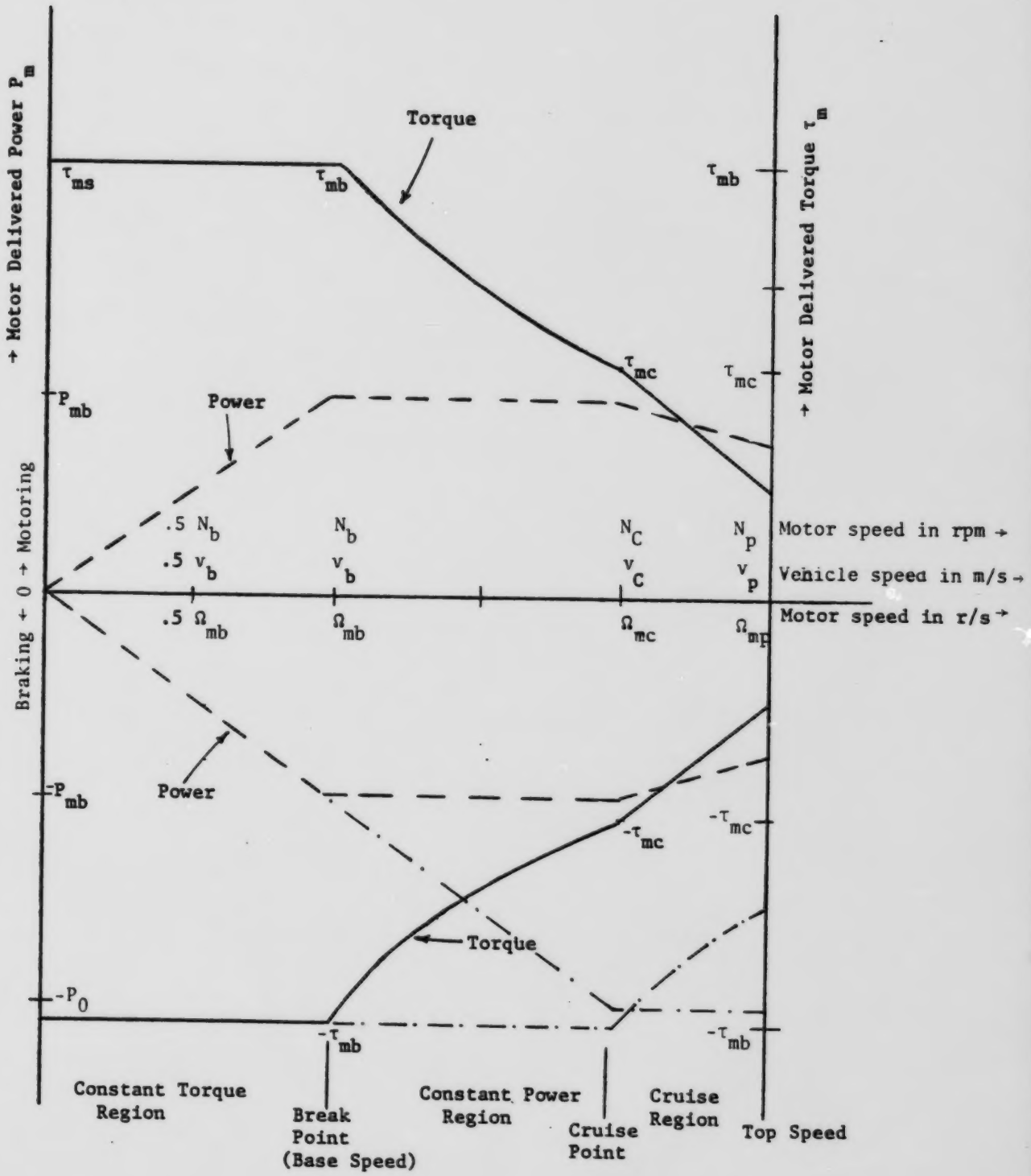


Figure 2.1 Generalized Torque and Power Profiles for a Traction Drive Used for Obtaining Test Results.

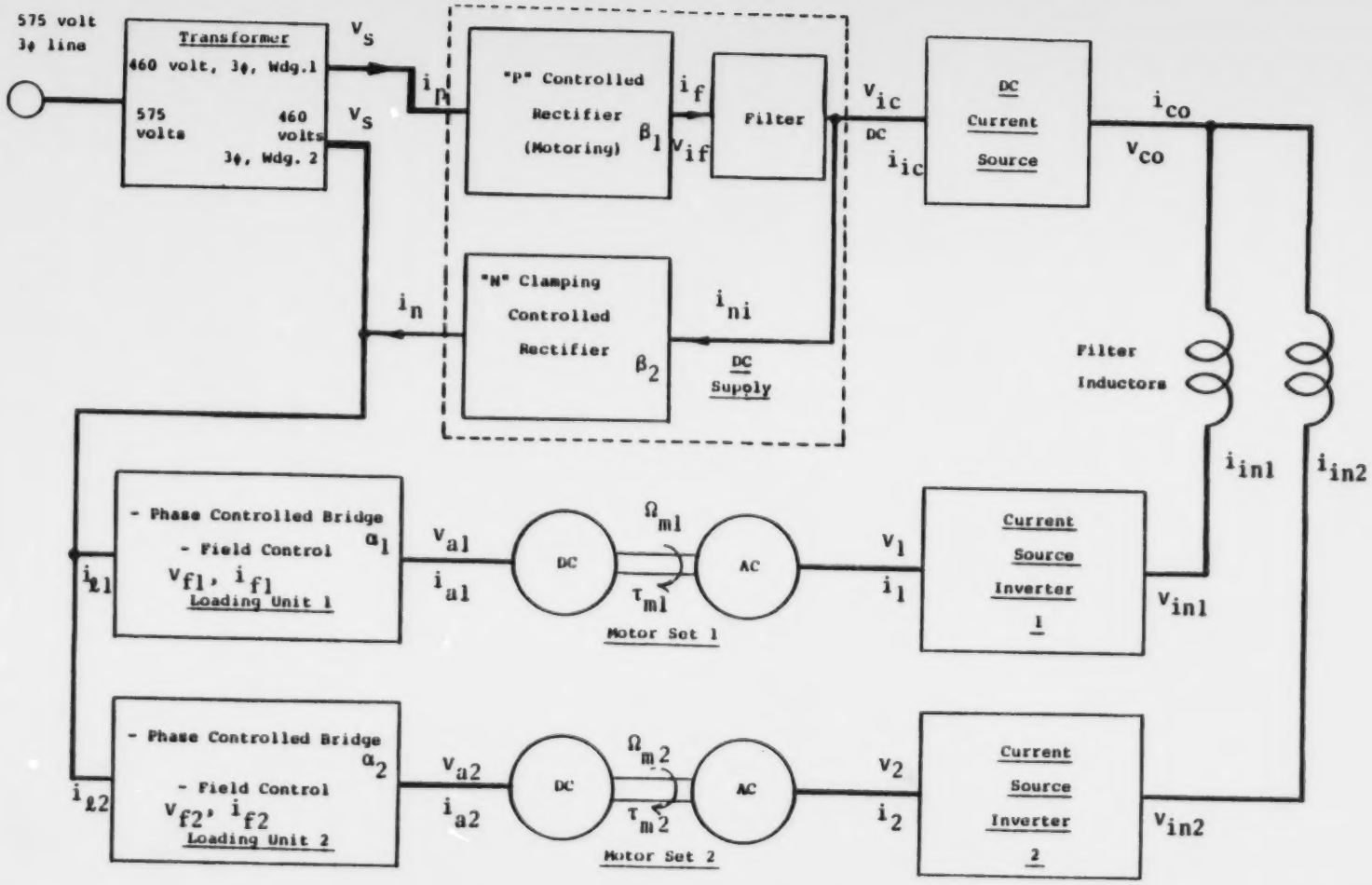


FIG. 2.2 - BLOCK DIAGRAM OF THE TWO MOTOR TEST SYSTEM SHOWING THE NOMENCLATURE (v and i represent inst. voltage and current respectively).

DC Supply Unit and Transformer

The dc power supply unit is capable of supplying or accepting 240 Kilowatts of power at 600 volts dc nominal (400 amperes) to operate the two-motor 250 HP ac propulsion system in both motoring and braking regions. The details of the dc supply unit and the transformer are described in Appendix A. This power supply unit consists of the following (Fig. 2.2):

(a) A three-phase controlled rectifier P operating in the rectifying mode with an output filter (inductor and capacitor). Under the normal operating conditions, the controlled rectifier operates with a delay angle β_1 nearly equal to zero (i.e., as an uncontrolled rectifier). The controlled rectifier (P) provides a controlled ramp charging of the filter capacitor and a protection if the current exceeds a preset value (provides a solid state contactor). The nominal rating of the unit is 600 volt dc and 400 amperes dc.

(b) A three-phase controlled rectifier N operating in the inverting mode with an output filter (inductor). Under the normal operating conditions, the controlled rectifier operates at a delay angle β_2 nearly equal to 180° (i.e., as a complete phase backed inverter). This inverter limits the dc voltage to a preset value when the system is being fed back with dc current up to 400 amperes (in the regeneration mode).

(c) Both the rectifier (P) and inverter (N) have: protection against drop of input ac and overcurrent, display of the output and input voltages and currents, all the relevant signals at logic levels in an isolated manner such that an interface with a data acquisition system can be made, and the capability such that the basic logic can be replaced with a microprocessor based logic system.

(d) The two rectifier units P and N are supplied from isolated 3-phase ac input to avoid large circulating current between P and N bridges in the dc link. The transformer designed has three-phase primary windings of 100 KVA at 575 volts and two secondary windings each capable to supply 400 KVA, three-phase at 460 volts. Several primary taps are available such that the secondary voltage can be adjusted ± 40%. The primary winding is air cooled and the secondary windings are water cooled. The main advantages of this transformer are:

i) The dc power supply can accept motoring or braking power up to 400 KVA from the secondary windings. The primary power is only the loss power and with 100 KVA power, drive systems up to 400 HP can be tested.

ii) All the loading and power supply units for the two motor tests are supplied from the secondary windings. As such only one transformer was needed for performing complete tests on the two motor system.

iii) The power interconnections between the test modules is greatly simplified.

DC Chopper Current Source

The chopper current source converts the dc input voltage to a dc current source which operates the current source inverters (240 Kilowatt for two motors) in both motoring and braking regions. The details of the chopper current source are presented in Appendix C.

This chopper is designed to operate from a nominal 600 volts dc bus and can produce output current of 400 amps and the output voltage can be controlled up to 600 volts dc in both positive and

negative directions. In this manner, the chopper can supply a current source inverter in both the motoring and braking regions. The unit is provided with meters for both input and output voltages and currents. This unit always operates at a fixed frequency (controlled by a crystal) and no frequency modulation is necessary at any point of operation on the traction torque speed curve. The on time of the chopper can be measured with a counter and the chopper can be operated in manual (on time control) as well as automatic current regulation mode. Some of the additional features of the design are:

(i) All the components are water cooled such that the chopper losses can be measured with water flow and temperature measurements.

(ii) Small signal logic protection is provided for lower limit of dc input voltage (avoids loss of commutation), higher limit of dc input voltages (avoids over-voltage across solid state power components) and overcurrent in the output (if regulating feedback loop has a malfunction).

Current Source Inverter

The overall test set-up requires (Fig. 2.2) two inverters each capable of providing 125 HP to the ac squirrel cage motor with both 230 volt and 460 volt 60 Hertz connections. The inverter frequency range is 0 to 150 Hertz (4000 rpm maximum motor speed) and the details of the inverter and instrumentation are described in appendix D. The inverter design is modular such that the value of the commutation capacitors can be changed easily. Some of the other features of the design are:

(1) All the major components are water cooled such that the system losses can be measured with water flow and temperature measurements.

(2) The logic is designed such that automatic gating of the inverter thyristors occurs if any overvoltage condition occurs. An over-

voltage protection in C.S.I. is necessary to avoid open connection or malfunction of the inverter with the resulting damage to the semiconductor components.

(3) The logic is designed such that both the slip frequency and power factor control can be tested by replacing a logic board. The system test results therefore were obtained both with the slip frequency and the power factor control.

(4) An instrumentation unit is designed which provides two isolated inverter output voltages with isolation amplifiers, two isolated phase current signals with Hall amplifiers, analog signal for the three phase power, analog signals for rms and fundamental output voltage and current, motor power factor and output frequency.

(5) The inverter can operate in all four quadrants of the speed-torque curve by small signal logic control. The reversal is achieved at zero current by modifying the inverter gating such that the output voltage phase sequence is reversed.

Loading Unit

The overall test set-up requires (Fig. 2.2) two loading units each capable of providing up to 125 Kilowatts to the separately excited dc machine (at 600 volts dc nominal) coupled to the 125 HP ac motor. A chopper unit for field control is also needed to obtain constant power loading in the constant power region of the speed-torque curve (Fig. 2.1). The loading unit is capable of loading the ac motor in both motoring and braking regions and the details of the unit are described in Appendix B.

The loading unit consists of the following:

(a) A three-phase controlled rectifier to supply the armature of the loading machine,

(b) Filter inductor,

(c) DC chopper to supply the field.

The input to the unit is three-phase, 460 volt and the outputs are dc voltages for armature and field (both are independently controllable). The continuous rating of the armature supply is 125 kW at 600 volts dc nominal and the field unit can supply up to 10 kW up to 600 volts dc. The loading unit designed incorporates the following features:

(a) Protection against drop of input ac, overcurrent in armature, loss of field current, etc.,

(b) Manual control and display of the output and input voltages and currents,

(c) All the relevant signals are brought down to logic levels in an isolated manner such that an interface with a data acquisition system can be made,

(d) The capability is provided such that the basic logic can be replaced with a microprocessor system,

(e) The capability of automatic control of the armature current and the armature voltage or speed (with inner current loop) has been provided,

(f) The capability of automatic control of the field current as a controlled function of the armature voltage can be implemented,

(g) The unit can provide static four quadrant loading with field reversal. Under dynamic conditions (field direction change in manual) only a two quadrant loading can be achieved.

2.3 Test Results

The test results, to achieve the basic objectives outlined in section 2.1, were conducted in steps outlined in this section. The quantities measured for the dc power supply unit, the chopper current source unit, the current source inverter unit and the loading unit are outlined in Tables 2.1, 2.2, 2.3 and 2.4 respectively. The typical torque speed profile used for the test results is shown in Figure 2.1.

STEP I - Single Motor Tests at Nominal Conditions with 460 Volt Motor Connection and 2:1 Constant Speed Range

The nominal design conditions with 4 pole, 460/230, 125 HP, 3 phase, 60 Hz ac squirrel cage motor are defined as follows (Figures 2.1 and 2.2);

V_{ic} = 600 volt = Chopper input dc voltage (2.1)

P_{mb} = Power at base speed = 100 kw (2.2)

N_b = 1800 rpm = Base motor speed (2.3)

N_c = 3600 rpm = Cruise point motor speed (2.4)

N_p = 4000 rpm = Maximum motor speed (2.5)

f_{rb} = Rated value = Brake point rotor frequency (2.6)

For the operating profile defined by equations 2.1 to 2.6, the maximum value of the current source commutation capacitor was determined to ensure stability (a higher commutation capacitance value results in a lower component rating as shown in reference 2). Also, the 'preferred' values of the chopper current source commutation components were determined to ensure a minimum loss of the chopper current source, reference [115] in Bibliography.

At the base speed (N_b) of the system operation, a detailed measurement of the waveforms and the component ratings of the chopper current source

and the current source inverter were carried out. The theoretical results obtained from references 1 and 2 were verified with the experimental results.

The results of the steady state operation were obtained from the basic system units (Tables 2.1, 2.2, 2.3 and 2.4) at the motor speed N equal to zero, .5 N_b, N_b, $(N_b + N_c)/2$ and N_p in both the motoring and braking regions of the typical torque speed diagram of Figure 2.1. These results were obtained with the following adjustment of the controls of the four basic units.

(i) Steady State results at N = 0, motoring

Rotor frequency $f_r = f_{rb}$ (rated positive value).

Chopper current I_{co} was adjusted to obtain the rated torque.

Field current I_{fl} of the loading unit was at the maximum positive value.

Armature current I_{al} of the loading unit was positive.

Armature voltage V_{al} was positive equal to $I_{al} R_{al}$ where R_{al} is the armature resistance.

Delay angle α_l of the loading unit was slightly less than 90^o and was adjusted to obtain the rated torque.

Two basic adjustments were I_{co} of the chopper and the delay angle α_l of the loading unit.

(ii) Steady state results at N = .5 N_b, motoring

Same conditions as (i) except that V_{al} of the loading unit was negative and α_l was greater than 90^o. The basic adjustments were I_{co} of the chopper current source and the delay angle α_l of the loading unit.

Table 2.1: Quantities measured on the dc supply unit at all the steady state operating points.

V_{ic} = Average dc chopper input voltage

I_{ic} = Average dc chopper input current.

i_{ic} = Instantaneous chopper input current.

I_{iq} = rms qth harmonic input chopper current.

I_f = Average output current of "P" controlled rectifier bridge.

I_{ni} = Average input current of "N" controlled rectifier bridge.

P_{ic} = Power input to chopper current source = V_{ic} (I_f - I_{ni})

Table 2.2: Quantities measured on the chopper current source unit at all steady state operating points

v_{co} = Instantaneous chopper output voltage.

V_{co} = Average output chopper voltage.

V_{cr} = rms rth harmonic chopper output voltage.

i_{co} = Instantaneous chopper output current.

I_{co} = Average chopper output current.

I_{cx} = rms xth harmonic chopper output current.

$P_{c\ell}$ = Chopper loss power (water flow loss and loss in chopper air cooled resistors).

P_{co} = Chopper output power = $P_{ic} - P_{c\ell}$

P_{ic} = Chopper input power from Table 2.1.

v_{cmt} = Peak chopper main thyristor voltage

v_{cct} = Peak chopper commutation thyristor voltage.

f_c = chopper frequency in Hertz.

Table 2.3: Quantities measured on the current source inverter units at all steady state operating points

i_{in1} = Instantaneous inverter input current.

I_{in1} = Average inverter input current.

I_{i1y} = rms yth harmonic inverter input current.

v_{in1} = Instantaneous inverter input voltage.

V_{in1} = Average inverter input voltage.

V_{i1z} = rms zth harmonic inverter input voltage.

v_1 = Instantaneous inverter output voltage.

V_{1n} = rms nth harmonic inverter output voltage.

i_1 = Instantaneous inverter output current.

I_{1n} = rms nth harmonic inverter output current.

$P_{i1\ell}$ = inverter power loss (loss by water measurements and loss in air cooled inverter resistors).

P_{i1} = Inverter output power.

v_{i1t} = Peak inverter thyristor voltage.

v_{i1d} = Peak inverter diode voltage.

v_{i1c} = Peak inverter capacitor voltage.

f_{i1} = Inverter frequency in Hertz.

NOTE: Suffix 1 applies to the inverter unit 1 and suffix 2 applies to the inverter unit 2. (i_{in2}, I_{in2}, I_{i2y}, v_{in2}, V_{in2}, V_{i2z}, v_2, V_{2n}, i_2, I_{2n}, $P_{i2\ell}$, P_{i2}, v_{i2t}, v_{i2d}, v_{i2c} and f_{i2})

Table 2.4: Quantities measured on the loading units at all steady state operating points

V_{a1} = Average output voltage.

α_1 = Delay angle of the phase controlled bridge.

I_{a1} = Average output current.

I_{f1} = Average field current.

τ_{m1} = Motor torque in Newton-meters.

Ω_{m1} = $2\pi N/60$ = motor speed in rad/sec.

P_{m1} = $\tau_{m1}\Omega_{m1}$ in watts.

P_{dc1} = Power input to dc machine = $V_{a1}I_{a1}$.

NOTE: Suffix 1 applies to the loading unit 1 and suffix 2 applies to the loading unit 2 (V_{a2}, α_2, I_{a2}, I_{f2}, τ_{m2}, Ω_{m2}, P_{m2} and P_{dc2})

(iii) Steady state results at $N = N_b$, motoring

Rotor frequency $f_r = f_{rb}$ (rated positive value)

Delay angle α_1 of the loading unit was maximum nearly 170^o.

Armature voltage V_{a1} was negative and I_{a1} was positive.

Two basic adjustments were I_{co} of the chopper current source and the positive field current I_{f1} of the loading unit.

(iv) Steady state results at $N = (N_b + N_c)/2$, motoring

Same adjustments in (iii) except that the rotor frequency = $f_{rb}(N_b + N_c)/(2N_b)$ and was positive.

(v) Steady state results at $N = N_c$, motoring

Same adjustments as in (iii) except that the rotor frequency $f_r = f_{rb}\ N_c/N_b$ and was positive.

(vi) Steady state results at $N = N_p$, motoring

Same adjustments as in (iii) except that the rotor frequency $f_r = f_{rb}\ N_p/N_b$ and was positive.

(vii) Steady state results at $N = 0$ and $N = N_b/2$, braking

Rotor frequency $f_r = -f_{rb}$ (rated negative value) field current I_{f1} of the loading unit was at the maximum negative value. Both I_{a1} and V_{a1} were positive. Two basic adjustments were I_{co} of the chopper current source and the delay angle α_1 (less than 90^o) of the loading unit.

(viii) Steady state results at $N = N_b$, braking

Rotor frequency $f_r = -f_{rb}$ (rated negative value).

Delay angle α_1 of the loading unit was at minimum (nearly zero).

Both V_{a1} and I_{a1} were positive.

Two basic adjustments were I_{co} of the chopper current source and the negative field current I_{f1} of the loading unit.

(ix) Steady state results at $N = (N_b + N_c)/2$, braking

Same adjustments as in (vii) except that the rotor frequency

$$f_r = - f_{rb} (N_b + N_c)/(2N_b).$$

(x) Steady state results at $N = N_c$, braking

Same adjustments as in (viii) except that the rotor frequency

$$f_r = -f_{rb}N_c/N_b.$$

(xi) Steady state results at $N = N_p$, braking

Same adjustments as in (viii) except that the rotor frequency

$$f_r = - f_{rb}N_p/N_b.$$

The dynamic tests were performed without using the loading unit. Both during acceleration (from zero to top speed) and braking (top speed to zero) the torque, speed and the key component specifications of the chopper current source and the current source were monitored. The results thus generated established the worst case voltages across the thyristors during the transient or dynamic conditions. To move from motoring to braking, the direction of the rotor frequency was changed from positive to negative. If a mechanical (flywheel) simulation of the vehicle was available, the results thus generated would predict the vehicle system dynamic performance by a mechanical simulation of the load. An attempt was made to obtain a theoretical dynamic model to predict the experimental results.

STEP II - Single Motor Tests at Nominal Conditions with 460 Volt Motor Connection and 3:1 Constant Power Region

Step I with N_b=1200 rpm, N_c=3600 rpm, N_p=4000 rpm and P_{mb}=100 kw was repeated. This step involved a new selection of the 'preferred' values of the commutation components of the chopper current source and the

current source inverter units. A comparison of the results from Step I and Step II illustrated the effects of altering the range of the constant power region.

STEP III - Single Motor Tests at Nominal Conditions with 230 Volt Motor Connection and 2:1 Constant Power Region

Step I with N_b=1800 rpm, N_c=3600 rpm and N_p=4000 rpm, P_{mb}=100 kw and 230 volt motor connection was repeated. This step involved a new selection of the 'preferred' values of the commutation components of the current source and the current source inverter units. A comparison of the results from Step I and Step III illustrated the effects of using lower motor voltage at the base speed of operation of the torque speed curve. These results were also used in Step IV for the series connection of the inverter for the two motor system simulation.

STEP IV - Two Motor Tests with 230 Volt Motor Connection and Series Connection of the Inverters

These test results were obtained at the nominal conditions with 2:1 constant power region. The design of the chopper current source and the current source units were the same as in Step III. All the results in Step I were repeated with zero, 10% and minus 10% speed differentials between the two ac motors.

STEP V - Two Motor Tests with 460 Volt Motor Connection and Parallel Connection of the Inverters

These test results were obtained at the nominal conditions in step I. The design of the chopper current source and the current source units were the same as in Step I. All the results in Step I were repeated with zero, plus 10% and minus 10% speed differentials between the two ac motors.

2.4 Conclusions

In obtaining the test results from the experimental drive system, problems of minor nature were encountered in the electronic circuitry. These problems were solved and it was observed that the drive system performance met all the desired specifications. The test results showed that essentially most of the requirements verified experimentally in [3] for a lower power drive system, also are valid for the higher power drive systems. A detailed comparison of the experiments and the results can be found in [3].

CHAPTER 3

DESIGN PROCEDURES

3. DESIGN PROCEDURES

3.1 Introduction

The summary of a basic design procedure for single- and multi-axle traction drive systems based on earlier reports [1]-[2], experiments and reference [3] is presented in this chapter. The recommended drive system consists of one 2-quadrant chopper current source unit whose chopping frequency is kept constant under all operating conditions and whose output voltage is regulated with an 'optimum' control strategy as explained in reference [3]. The chopper current source feeds one or two current source inverters with an adjustable dc current. At the last stage each inverter drives a squirrel cage induction motor.

The drive system design procedure starts by specifying the traction drive requirements described in Section 3.2. The selection of an appropriate induction machine for a single-axle system is covered in section 3.3. Section 3.4 gives the details of the design of a current source inverter based on the specifications of the selected machine. Besides, the motor selection and the design procedure for the case of two series or parallel inverters are also included in this section. Finally, Section 3.5 shows the steps to be taken in order to design a chopper current source capable of delivering the demanded power to the current source inverter(s).

3.2 General Characteristics of Traction Drives

The basic block diagram of a traction drive system is shown in Fig. 3.1. The system consists of

(a) Power Source: The required power source for a traction application may be on board or off board. In the former case, e.g., in locomotives, the power source is considered as a part of the power conditioner described in the following. In the other case the power source may be either an ac pickup with an on board rectifier or a dc bus consisting of a "third rail" or overhead wires. The power source is generally specified as to the following parameters:

(1) ac or dc

(2) Nominal voltage

(3) Voltage variation (in % of nominal)

(4) Transient voltage peaks

(5) Regenerative receptivity

(6) Allowable harmonic currents (in % of line current)

(b) Power Conditioner: This system produces the appropriate voltage, current and frequency profile so as to create the required torque-speed characterisitcs from the drive motor(s). Typical torque-speed characteristics are shown in Fig. 3.2. In general, traction drives have the following operating modes:

(1) A constant torque mode, from standstill to break (base) speed, v_b.

(2) A constant power mode, from break (base) speed to cruise speed, v_c.

(3) A cruising mode, from cruise speed to peak speed, v_p.

For some applications, the above three modes are identical for both motoring and braking operations. Other applications, however, require that full braking torque be available up to the cruise speed.

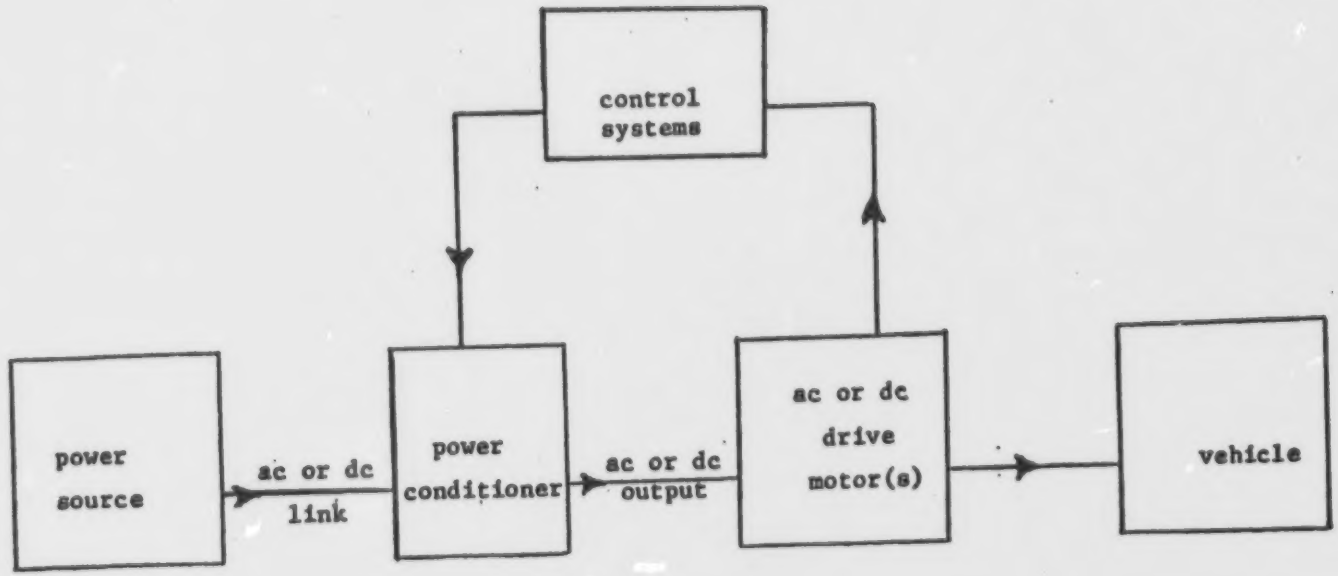


Figure 3.1 Basic Block Diagram of a Traction Drive System

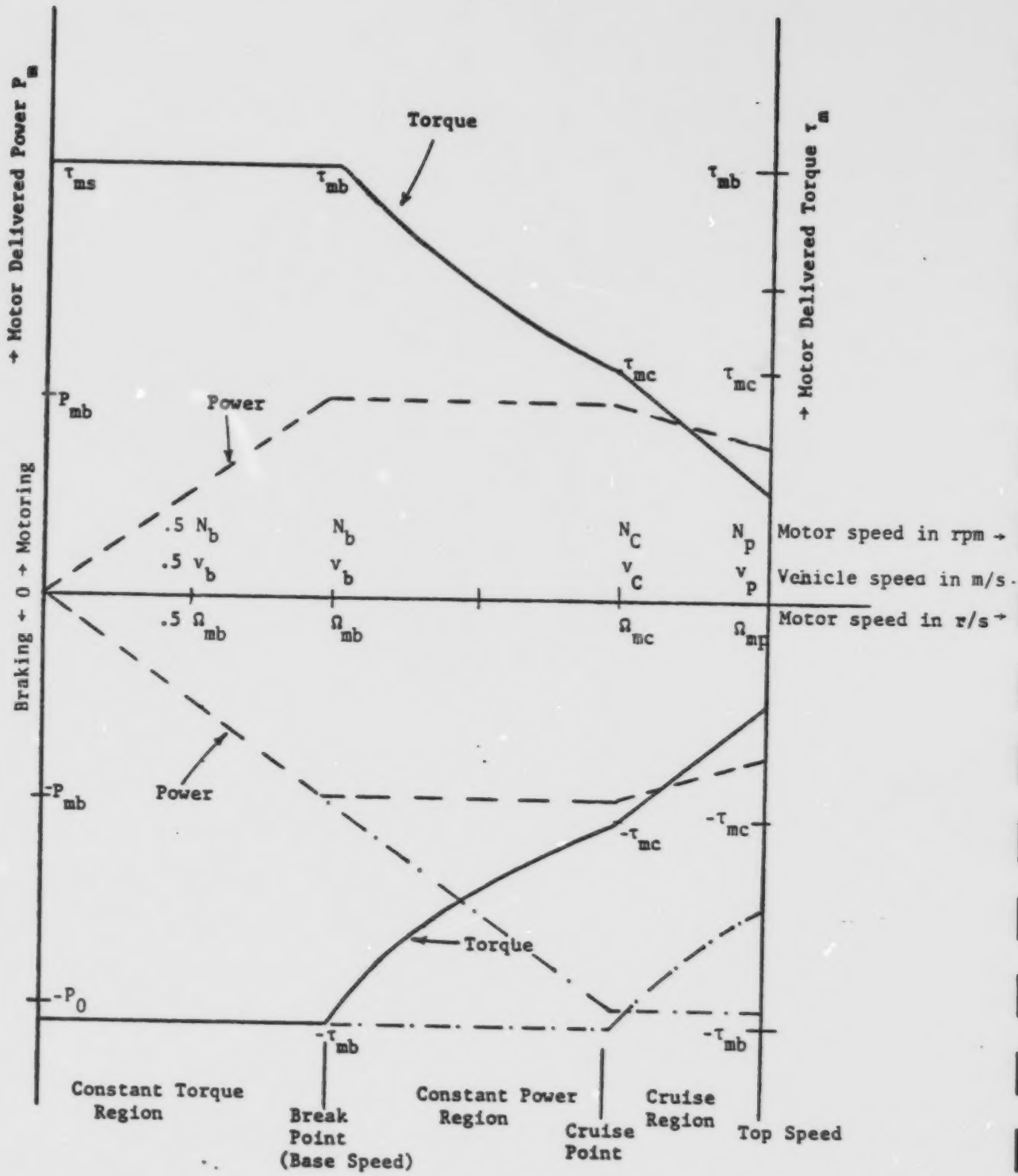


Figure 3.2 Generalized Torque and Power Profiles for a Traction Drive Used for Obtaining Test Results.

In these cases, the required braking power at the cruise point is determined by the expression,

$$P_o = P_{mb} \cdot v_c/v_b \qquad (3.1)$$

where P_{mb} is the peak motoring power at the break point.

The power profile shown in Fig. 3.2 indicates the peak power requirements of the motor(s) as a function of speed. The peak power rating for the power conditioner is then equal to the larger instantaneous motor power, P_{mb} or P_o. However, the conditioner is not generally required to deliver this power level continuously. The continuous power rating is determined by averaging the instantaneous power requirements over a typical operating cycle.

In specifying the power conditioner only the machine characteristics at standstill, break point, cruising point and top frequency point, for both motoring and braking modes, are required. The necessary machine characteristics at each operating point are:

(1) voltage

(2) current

(3) frequency

(4) effective machine parameters

The above characteristics can only be determined once the machine has been selected.

The power conditioner must also be coordinated with the power source characteristics, which are:

(1) Regenerative capability

(2) Nature of source, ac or dc

(3) Nominal voltage

(4) Voltage range for full power

(5) Voltage range for reduced power

(6) Harmonic current restrictions

If the power source is not fully receptive, the excess regenerated power is dissipated in braking resistors which would then have to be included as part of the power conditioner.

The power conditioner is specified as to the following parameters:

(1) Power source characteristics as described above

(2) Machine characteristics as described above

(3) Continuous power rating

(4) Peak power rating

(5) Required braking power

(6) Signalling and/or communication interference restrictions

(7) Size limitations

(8) Weight limitations

(9) Humidity range

(10) Temperature range

(11) Acceleration stresses in all three directions

(12) Minimum MTBF (Mean Time Between Failure)

(c) Drive Motor(s): The drive system may consist of a single motor or several motors, each mounted on a separate axle. The main requirement for each motor is that it produce the torque and power profiles shown in Fig. 3.2. The rated motor power and speed are respectively equal to the motoring power and the required shaft rpm at the break point.

For multi-axle drives with squirrel cage induction motors it is necessary to estimate the differential speed between axles. This can be determined from the maximum allowable differential wear between wheel diameters.

The drive motors are generally specified as to the following parameters:

(1) Number of motors per vehicle

(2) Power rating of each motor (continuous and 1 hour peak)

(3) Motor rpm at break, cruise and top speed, points

(4) Motor size constraints

(5) Class of insulation

(6) Temperature range

(7) Humidity range

(8) Acceleration stresses in each of three directions

(9) Minimum MTBF (Mean Time Between Failure)

(10) Maximum differential wheel wear

(d) Control Systems: This part of the drive system consists of the interface between the operator and the power conditioner, the wheel slip control (anti-skid control) systems, circuit breakers and fuses, fault indicators, and diagnostics and gauges.

The control systems can be specified as to the following parameters:

(1) Thrust control or speed control

(2) Braking only when brake command is activated, or braking as soon as acceleration command is released

(3) Maximum acceleration and/or deceleration

(4) Parameters to be sensed by wheel slip control

(5) Procedure to be activated by wheel slip control

(6) Maximum circuit breaker and fuse ratings

(7) Limit on number of breaker resets

(e) Vehicle: Some of the vehicle specifications have already been considered for other parts of the drive systems, i.e.:

(1) Size and weight limitations for the motor and power conditioner

(2) Temperature and humidity range for motor and power conditioner

(3) Acceleration stresses for motor and power conditioner.

The other required information is:

(4) Type of vehicle (trolley coach, subway car, light rail or commuter locomotive, freight locomotive)

(5) Maximum and minimum mass of the vehicle

(6) Nature of on board auxiliary power supplies

3.2.1 Summary of the Specifications of a Traction Drive System

The following list specifies the items whose values or descriptions are necessary for designing a traction drive system. Note that some of these items may not be applicable to some vehicles.

(a) Power source

(1) ac or dc

(2) Nominal voltage

(3) Voltage variation

(4) Transient voltage peaks

(5) Regenerative receptivity

(6) Allowable harmonic current

(b) Power conditioner

(1) Voltage range (operating range, full power range)

(2) Continuous power rating

(3) Peak power rating (1 hour)

(4) Required braking power

(5) Signalling/communications bands

(6) Size

(7) Weight

(8) Humidity range

(9) Temperature range

(10) Acceleration stresses (vertical, axial, lateral)

(11) MTBF (Mean Time Between Failure)

(c) Drive motor(s)

(1) Number of motors

(2) Power rating

(3) rpm (break, cruise, top speed, points)

(4) Size

(5) Weight

(6) Class of insulation

(7) Temperature range

(8) Humidity range

(9) Acceleration stresses (vertical, axial, lateral)

(10) MTBF

(11) Differential wheel wear

(d) Control system

(1) Thurst or speed control

(2) Braking activation

(3) Maximum acceleration/deceleration

(4) Parameters sensed by wheel slip control (absolute and/or relative wheel speed, absolute acceleration)

(5) Procedures activated by wheel slip control (initiation of sanding, reduction of motor excitation, initiation of braking)

(6) Breakers, fuses, etc.

(7) Number of breaker resets

(e) Vehicle

(1) Type

(2) Total mass (with passengers)

(3) Auxiliary power

3.3 Squirrel-Gage Induction Motor Selection

In this section a procedure is established for selecting an appropriate squirrel cage machine for any traction application. The selection is based on a monomotor system. The same procedure can be used for a multi-motor drive if each motor is powered from a separate inverter. The control strategy chosen is the slip frequency control whereas other control strategies (power factor control, current limit control) may also be considered [1].

The following steps determine the basic machine ratings:

(1) Specify the dc voltage of the power supply (chopper input voltage), V_{ic}.

(2) Neglecting all the losses in the system, calculate the maximum inverter input current for the machine maximum output power at base speed, P_{mb} (Figs. 2.1 and 2.2):

$$I_{inb} = P_{mb}/V_{ic} \tag{3.2}$$

(3) Calculate the machine rms fundamental harmonic of current at base speed:

$$I_{1b} = .78 I_{inb} = .78\ P_{mb}/V_{ic} \tag{3.3}$$

(4) Select the number of machine poles equal to 4.

(5) Select an induction machine capable of providing the required power at base speed, P_{mb}, with a rated input current around the value given in Eq. (3.3). Specify the machine parameters from the manufacturer's data sheet.

(6) The rotor, bearings, tolerances, etc., of the selected machine must be rated for the top speed, Ω_{mp}.

(7) Sketch the machine, torque, phase voltage and power factor, curves versus slip frequency, ω_r, for the stator base frequency, ω_{ib}, and current, I_{1b}, assuming the machine excited by a current

source inverter and using the following expressions. Note that the power factor and torque, curves are independent of the stator frequency. The typical curves are shown in Fig. 3.3.

$$R_{in} = \frac{R_r}{\omega_r}\omega_{ib}\frac{L_m^2}{(R_r/\omega_r)^2 + (L_m + L_r)^2} \tag{3.4}$$

$$X_{in} = \omega_{ib}\left[L_s + L_m \frac{(R_r/\omega_r)^2 + L_r(L_m + L_r)}{(R_r/\omega_r)^2 + (L_m + L_r)^2} \right] \tag{3.5}$$

$$Z_{in} = R_{in} + jX_{in} \tag{3.6}$$

$$V_1/\sqrt{3} = I_{1b} \cdot |Z_{in}| \tag{3.7}$$

$$\tau_e = \frac{3p}{2}\frac{R_r\omega_r L_m^2}{[R_r^2 + \omega_r^2(L_r + L_m)^2]} \cdot I_{1b}^2 \tag{3.8}$$

$$\text{Cos}\phi_{in} = R_{in}/|Z_{in}| \tag{3.9}$$

where

R_r = Rotor resistance per phase referred to stator, Ω

L_s = Stator leakage inductance per phase, H

L_r = Rotor leakage inductance per phase referred to stator, H

L_m = Magnetizing inductance per phase referred to stator, H

ω_{ib} = Stator frequency at base speed, rad/s

ω_r = Slip frequency, rad/s

R_{in} = Machine total equivalent resistance per phase, Ω

X_{in} = Machine total equivalent reactance per phase, Ω

Z_{in} = Machine total equivalent impedance per phase, Ω

$V_1/\sqrt{3}$ = Machine input voltage per phase, V

I_{1b} = Stator rms fundamental harmonic of current at base speed (Eq. 3.3), A

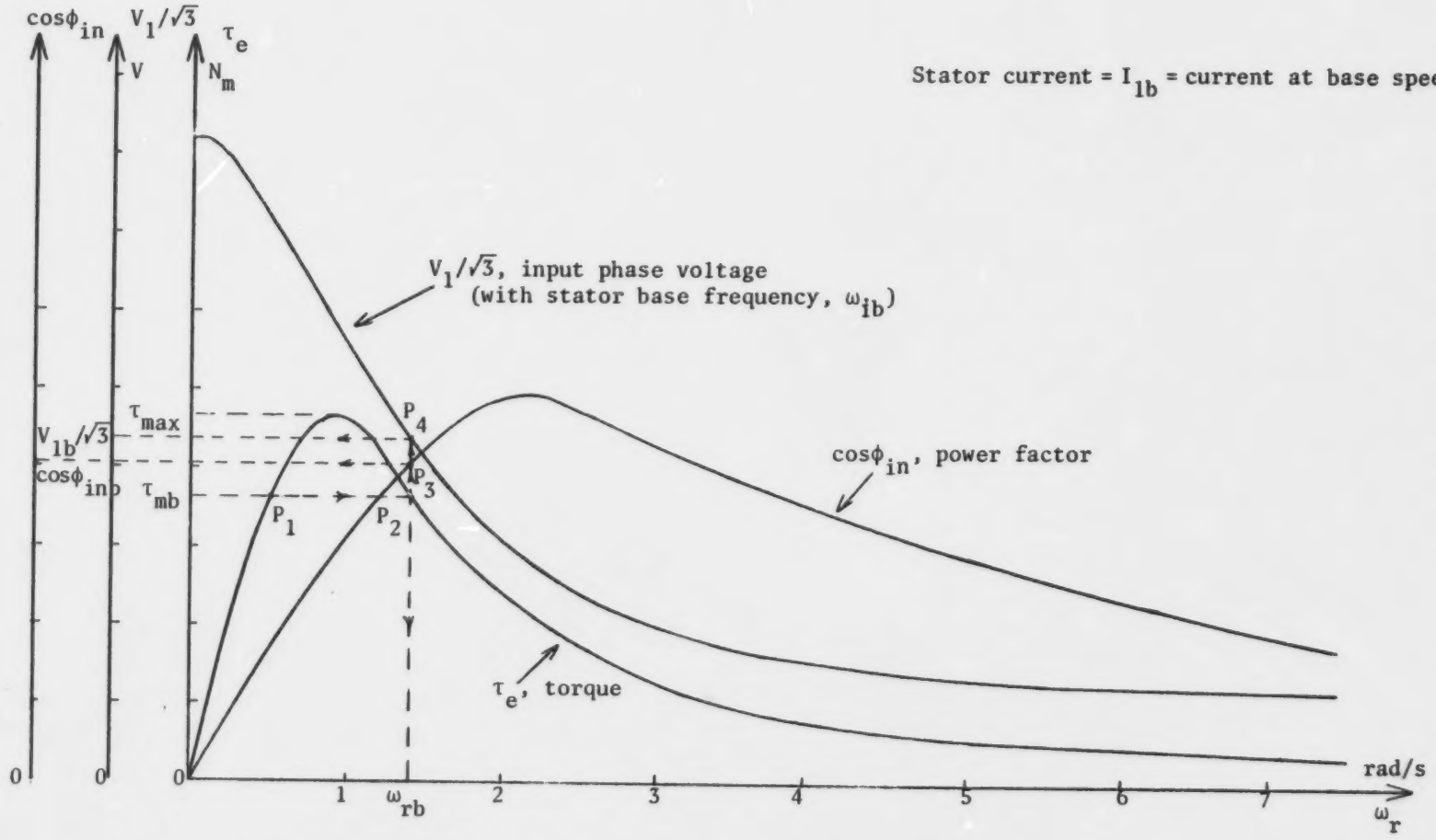


Figure 3.3 Squirrel-Cage Induction Machine Phase Voltage, Power Factor and Electromagnetic Torque, Typical Curves Versus Slip Frequency at Base, Stator Current, I_{1b}, and Frequency, ω_{ib}, for the Case that the Machine is Excited by a Current Source Inverter.

τ_e = Machine total electromagnetic torque, Nm

p = Machine number of poles

$\cos\phi_{in}$ = Machine power factor

(8) Compare the required peak torque at the break point, τ_{mb}, given in Fig. 3.2 with the maximum available torque, τ_{max}, on the torque versus slip frequency curve sketched in step (7) above (similar to Fig. 3.3). For a satisfactory operation τ_{max} must be larger than τ_{mb}. If not, select another machine and go back to step (7).

(9) In the constant torque region of Fig. 3.2 both the machine input current and the slip frequency are kept constant and equal to their corresponding values at base speed, I_{1b}, ω_{rb}, respectively. Determine the value of ω_{rb} by finding the corresponding slip frequency for the torque at base speed, τ_{mb}, from the torque/slip frequency curve plotted in step (7). Select the point with a higher power factor, point P_2 in Fig. 3.3. The machine phase voltage, $V_{1b}/\sqrt{3}$, and power factor, $\cos\phi_{inb}$, at base speed are also found from the curves in Fig. 3.3, points P_3 and P_4. At base speed the following expression must hold,

$$1.35\ V_{1b}\ \cos\phi_{inb} \leq V_{ic} \qquad (3.10)$$

If not, choose another machine and go back to step (7). Note that the machine input voltage in the constant torque region is a linear function of stator frequency, ω_i.

(10) In the constant power region the motor output power is kept constant and equal to its value at base speed, P_{mb},

$$P_{mb} = 3I_{1b}^2 R_r \frac{\Omega_{mb}}{\omega_{rb}} \frac{L_m^2}{(R_r/\omega_{rb})^2 + (L_m + L_r)^2} \qquad (3.11)$$

where I_{1b}, Ω_{mb} and ω_{rb} are respectively the stator current, shaft frequency and slip frequency all at base speed. The variation of slip frequency, ω_r, versus per unit shaft speed, Ω_m/Ω_{mb}, in the constant power region is obtained from the following expression:

$$\omega_r = K_1 \left(\frac{\Omega_m}{\Omega_{mb}} \right) + \left\{ K_1^2 \left(\frac{\Omega_m}{\Omega_{mb}} \right)^2 - \frac{R_r^2}{(L_m + L_r)^2} \right\}^{.5} \qquad (3.12)$$

where

$$K_1 = \frac{\omega_{rb}}{2} \left\{ \frac{R_r^2}{\omega_{rb}^2 (L_m + L_r)^2} + 1 \right\}$$

Fig. 3.4 shows a typical curve of the variation of slip frequency, ω_r, versus the per unit shaft speed, Ω_m/Ω_{mb}. Note that in the constant power region I_1 is kept constant and equal to its value at base speed, I_{1b}.

(11) The per unit variation of the machine line voltage in the contant power region is obtained from,

$$V_1 \text{ (p.u.)} = \frac{V_1}{V_{1b}} = \frac{\text{Cos}\phi_{inb}}{\text{Cos}\phi_{in}} \cdot \frac{1-S_b}{1-S} \simeq \frac{\text{Cos}\phi_{inb}}{\text{Cos}\phi_{in}} \qquad (3.13)$$

where V_1 and $\text{Cos}\phi_{inb}$ are the machine, line voltage and power factor at base speed. Also in the above equation s_b is the machine slip at the base speed and $\text{Cos}\phi_{in}$ is the machine power factor at speeds higher than the base speed determined in the following way: (a) Obtain the slip frequency using either Eq. (3.12) or the corresponding curve in Fig. 3.4; (b) the

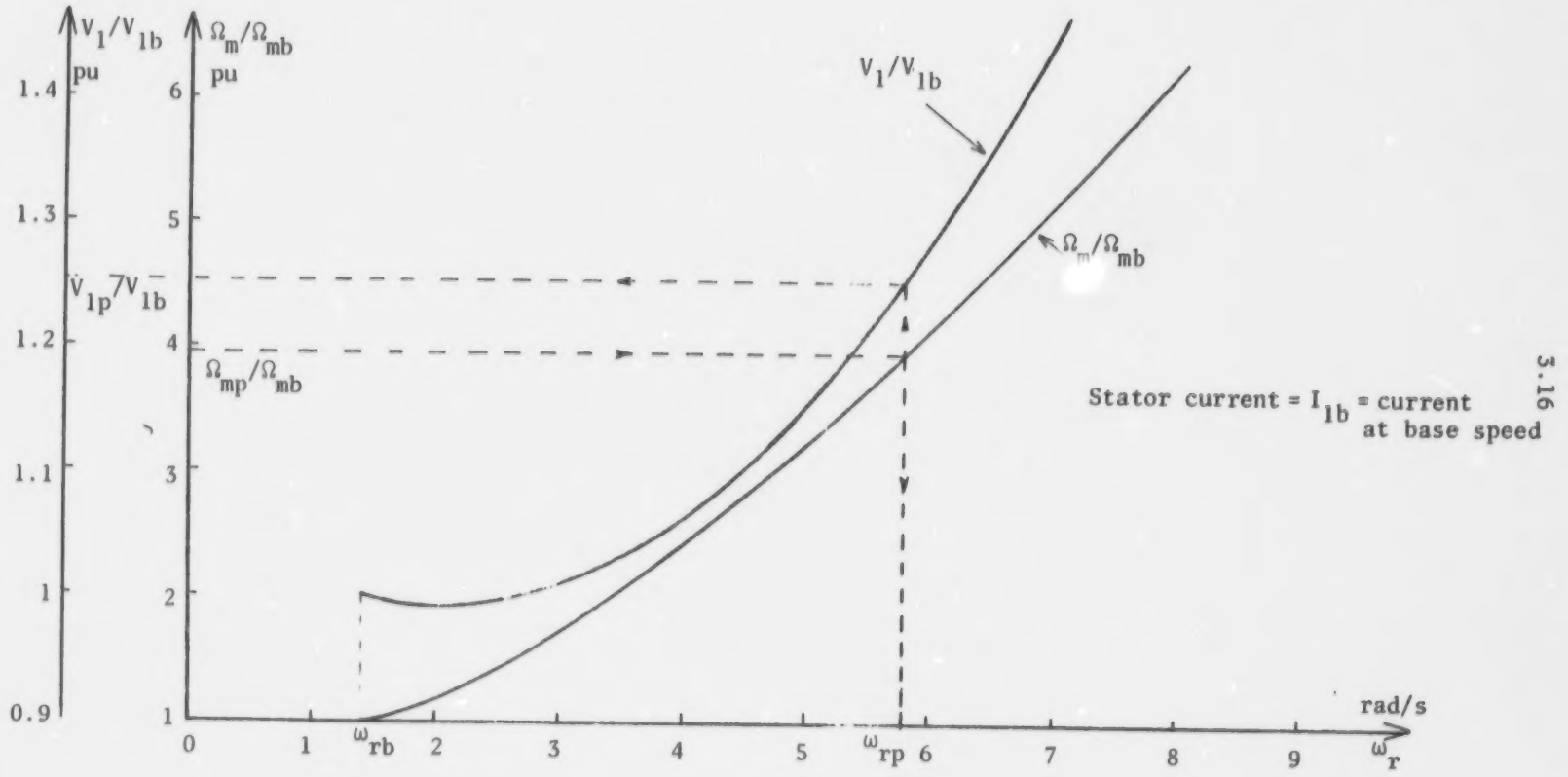


Figure 3.4 Squirrel-Cage Induction Machine Typical Curves of Per Unit, Shaft Speed and Line Voltage Versus Slip Frequency in the Constant Power Region and with Stator Current at Base Speed, I_{1b}. The Machine is Driven by a Current Source Inverter.

stator frequency would then be $\omega_i = \Omega_m + \omega_r$; (c) the values of ω_r and ω_i determined in (a) and (b) are inserted into Eqs. (3.4) and (3.5) in step (7) through which the required power factor, $\text{Cos}\phi_{in}$, is calculated from Eq. (3.9). A typical variation of motor line voltage in per unit for constant power region is also shown in Fig. 3.4.

(12) Obtain the ratio of the machine line voltage at its peak speed (Ω_{mp} in Fig. 3.2) to its value at base speed, V_{lp}/V_{lb}, from the corresponding curve in Fig. 3.4. Determine the value of V_{lp} knowing V_{lb} from step (9). The selected machine must be capable of withstanding this peak voltage.

3.4 Current Source Inverter Design

After selecting an induction machine capable of providing the traction drive system the requirements imposed by Fig. 3.2, a current source inverter should be designed such that it can supply both the continuous and the maximum power required by the induction machine. Depending on the system specifications, the inverter design is performed for the following two cases.

3.4.1 Inverter Design for a Single-Motor Drive System

This case applies to a single-axle traction vehicle. Fig. 3.5 shows the block diagram and the equivalent circuit of a single motor drive system [3]. The power circuit of an auto-sequentially commutated current source inverter is shown in Fig. 3.6. The detailed operation of the inverter is given in [3]. The following steps summarize the inverter design procedure:

(1) The maximum inverter input, voltage, V_{in} and current, I_{in}, are respectively equal to the voltage of power supply, V_{ic} (Fig. 3.5), and the maximum inverter input current at base speed, I_{inb}.

(2) Specify the maximum shaft speed, Ω_{mp}, using Fig. 3.2.

(3) Find the slip frequency at maximum shaft speed, ω_{rp}, from Eq. (3.12) in which Ω_{mp} found in step (2) above is substituted for Ω_m.

(4) The capacitance of the commutation capacitors in Fig. 3.6 is approximately calculated from,

$$C = \frac{0.1521}{\Omega_{mp}^2 L_\ell} \{(y^2 + 1.21y)^{0.5} - y\}^2 \qquad (3.14)$$

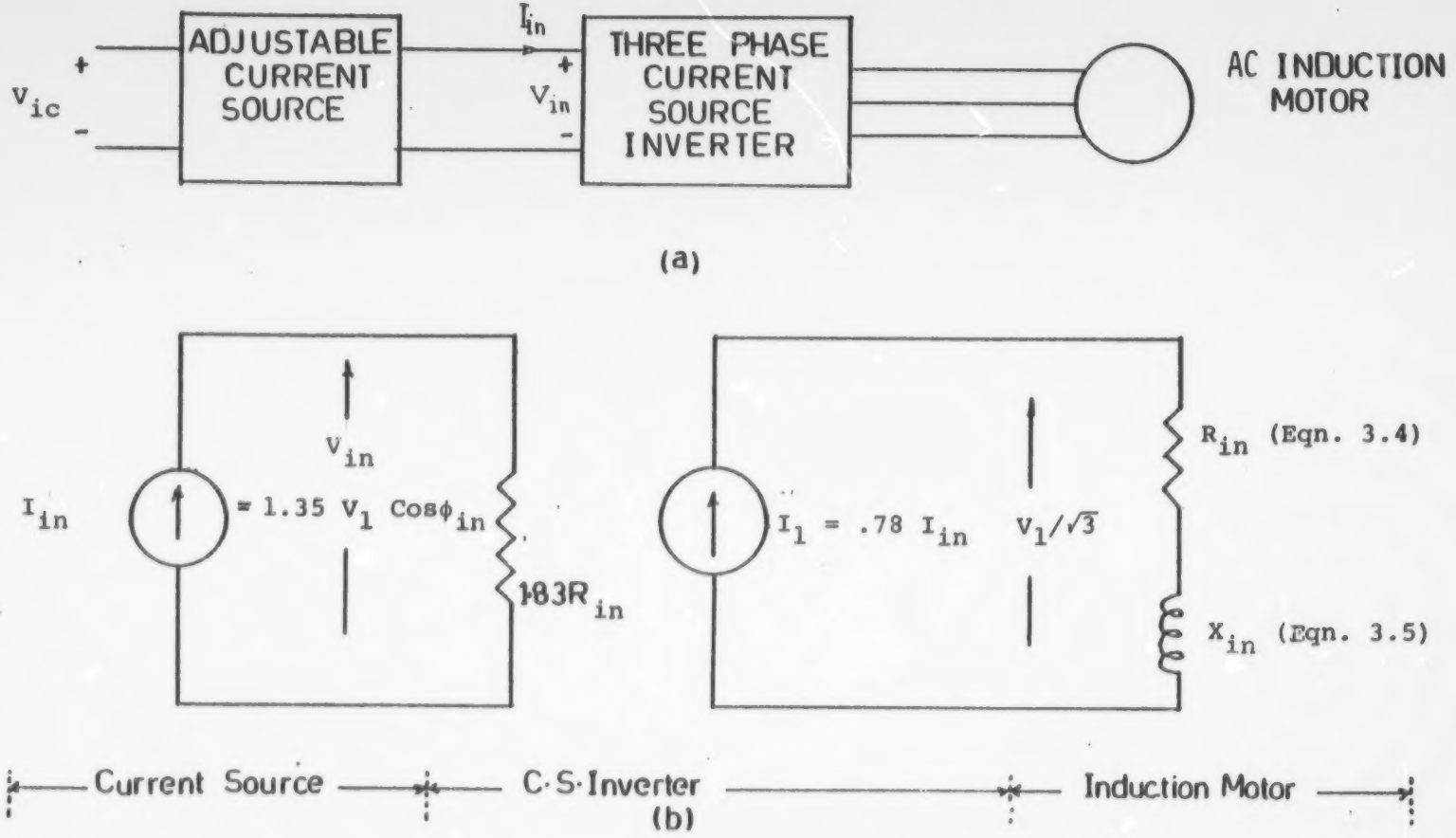


Fig. 3.5 (a) Block diagram of the current source inverter drive
(b) Equivalent circuit model for the C.S.I. drive.

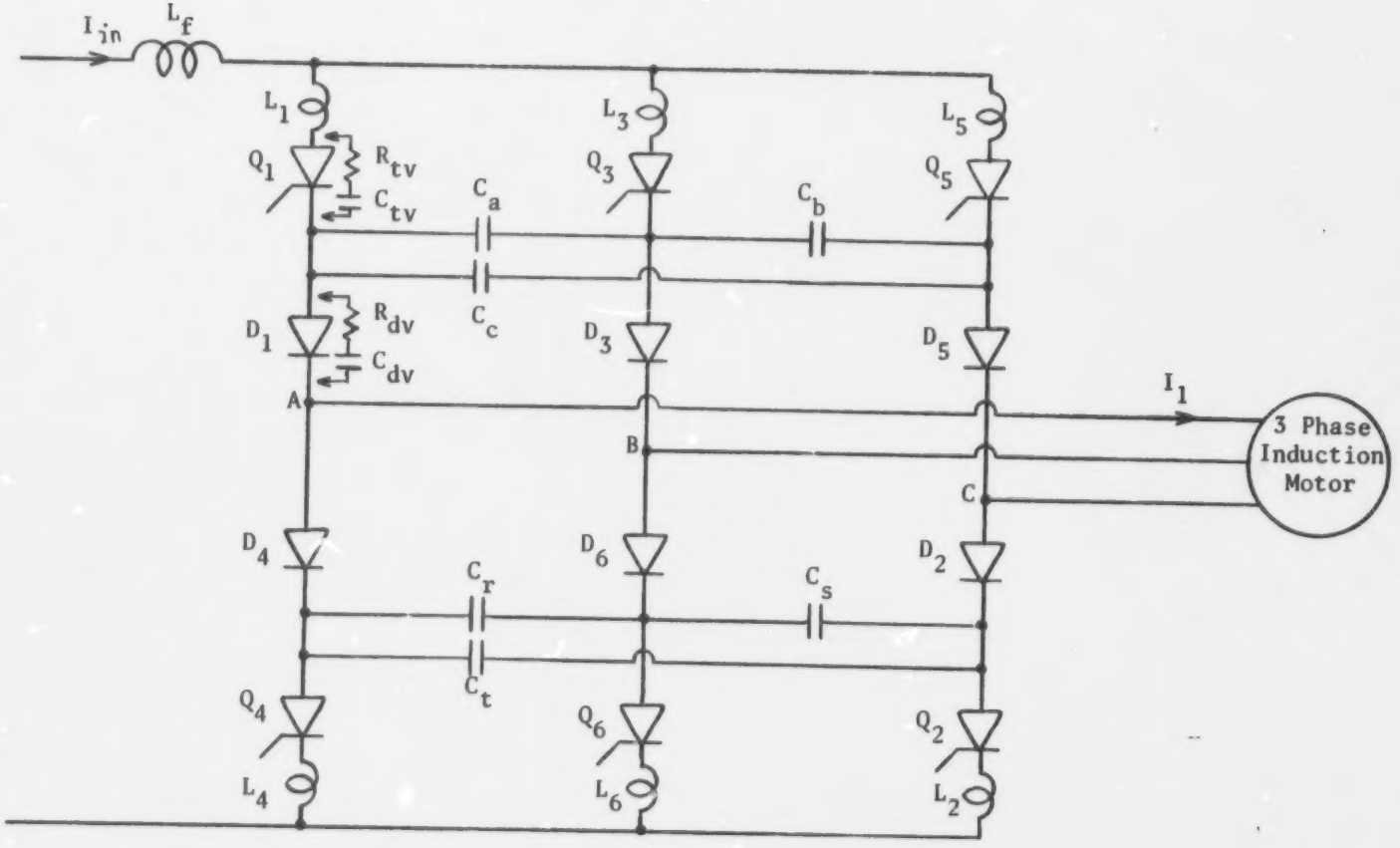


Fig. 3.6 Power circuit of an auto-sequentially commutated current source inverter.

where

$$y = L_\ell / L_b \tag{3.15}$$

$$L_\ell = L_s + L_r \tag{3.16}$$

$$L_b = \frac{(R_r/\omega_{rp})^2 (L_m - L_r) - L_r^2 (L_m + L_r)}{(R_r/\omega_{rp})^2 + (L_m + L_r)^2} \tag{3.17}$$

in which L_s, L_r, L_m and R_r are the motor parameters defined in step (7) of section (3.3) and ω_{rp} was found in step (3) above. Note that under no operating point should the selected capacitance for commutation capacitors result in a transient forward biasing of the series diodes in Fig. 3.6 [3].

(5) Obtain the peak voltage across commutation capacitors:

$$V_{ilc} = \sqrt{3}\, E_1 + \frac{2}{3} \frac{I_{inb}}{\omega_o C} \tag{3.18}$$

where

$$E_1 = I_{1b} \cdot |Z_{eb}| \tag{3.19}$$

$$Z_{eb} = R_{eb} + jX_{eb} \tag{3.20}$$

$$R_{eb} = \omega_{ib} \frac{(R_r/\omega_{rb}) \cdot L_m^2}{(R_r/\omega_{rb})^2 + (L_m + L_r)^2} \tag{3.21}$$

$$X_{eb} = \omega_{ib} \frac{(R_r/\omega_{rb})^2 (L_m - L_r) - L_r^2 (L_m + L_r)}{(R_r/\omega_{rb})^2 + (L_m + L_r)^2} \tag{3.22}$$

$$\cos \phi_{eb} = R_{eb} / |Z_{eb}| \tag{3.23}$$

$$\omega_o = 1/\sqrt{3L_\ell C} \tag{3.24}$$

In the above expressions I_{inb} and I_{1b} are the inverter input and stator currents at base speed given by eqns. (3.2) and (3.3) in section 3.3, ω_{ib} being the stator frequency at base speed (shaft speed equal to Ω_{mb} in Fig. 3.2), ω_{rb} is the slip frequency at base speed found in step (9) in section 3.3, C is the value determined in step (4) above, R_r, L_m, L_r, L_s the motor parameters and $L_\ell = L_s + L_r$.

(6) Calculate the peak rms value of the capacitor current,

$$I_C = I_{inb}[(2\theta_1+\theta_2)/(6\pi)]^{0.5} \tag{3.25}$$

where

$$\theta_1 = \frac{3}{2}\frac{\omega_{ip}\cdot C}{I_{inb}}(\sqrt{3}\,E_1' + V_{ilc}') \tag{3.26}$$

$$E_1' = I_{1b}\cdot|\,Z_{ep}\,| \tag{3.27}$$

$$Z_{ep} = R_{ep} + jX_{ep} \tag{3.28}$$

$$R_{ep} = \omega_{ip}\frac{(R_r/\omega_{rp})L_m^2}{(R_r/\omega_{rp})^2+(L_m+L_r)^2} \tag{3.29}$$

$$X_{ep} = \omega_{ip}\frac{(R_r/\omega_{rp})^2(L_m-L_r)-L_r^2(L_m+L_r)}{(R_r/\omega_{rp})^2+(L_m+L_r)^2} \tag{3.30}$$

$$\theta_2 = \omega_{ip}\left(\frac{\pi}{2}\sqrt{3L_\ell C}\right) \tag{3.31}$$

$$V_{ilc}' = \sqrt{3}\,E_1' + \frac{2}{3}\frac{I_{inb}}{\omega_o C} \tag{3.32}$$

in which ω_{ip}, ω_{rp} are respectively the peak stator frequency and the corresponding slip frequency. The other variables were defined in step (5) above.

(7) The thyristor ratings in Fig. 3.6 are as follows:

$$\text{Average thyristor current, } I_{tav} = I_{inb}/3 \qquad (3.33)$$

$$\text{rms thyristor current, } I_{tr} = I_{inb}/\sqrt{3} \qquad (3.34)$$

$$\text{Peak thyristor forward/reverse voltage, } V_{ilt} = 1.15\, v_{ilc} \quad (V_{ilc} \text{ from eqn. 3.18}) \qquad (3.35)$$

$$\text{Turn-off time, } t_q < \sqrt{3L_\ell C} \qquad (3.36)$$

(8) The series diodes ratings in Fig. 3.6 are obtained from the following expressions:

$$\text{Average diode current, } I_{dav} = I_{inb}/3 \qquad (3.37)$$

$$\text{rms diode current, } I_{dr} = I_{inb}/\sqrt{3} \qquad (3.38)$$

$$\text{Peak diode reverse voltage} = V_{ild} \simeq 2\, V_{ilc} \qquad (3.39)$$

(9) The thyristor di/dt protective inductances $L_i = L_1 - L_6$ in Fig. 3.6 are found as follows:

$$L_i \geq V_{ilc}/(di/dt)_{max} \qquad (3.40)$$

where V_{ilc} was given in step (5) and $(di/dt)_{max}$ is found from the manufacturer's data sheet for the thyristor selected in step (7). The chosen value of L_i should also be coordinated with the values of the thyristor snubber components in the next step.

(10) The snubber, resistance, R_{tv}, and capacitance, C_{tv}, across each thyristor in Fig. 3.6 are chosen in the following way.

$$R_{tv} = 2\sqrt{3L_i/C_{tv}} \tag{3.41}$$

$$(R_{tv})_{min} < R_{tv} < 0.5\ V_{ilc}/I_{rr} \tag{3.42}$$

$$I_{rr} \simeq \sqrt{2Q_{rr}(di/dt)} \tag{3.43}$$

where $(R_{tv})_{min}$ is the value of the snubber resistance recommended by the thyristor manufacturer, V_{ilc} is the value obtained in step (5), Q_{rr} is the device recovery charge given in the manufacturer's data sheet and $(di/dt) = V_{ilc}/(2L_i)$.

The values of R_{tv}, C_{tv} and that of L_i in step (9) should be selected in accordance with eqns. (3.40), (3.41) and (3.42).

(11) The series diode snubber, resistance, R_{dv}, and capacitance, C_{dv}, are selected such that

$$R_{dv} = 2\sqrt{2L_\ell/C_{dv}} \tag{3.44}$$

$$R_{dv} > (R_{dv})_{min} \tag{3.45}$$

where $(R_{dv})_{min}$ is the specified snubber resistance by the device manufacturer and $L_\ell = L_s + L_r$.

(12) The filter inductor L_f in Fig. 3.6 is selected to be approximately 3 to 5 times the sum of the stator and rotor leakage inductances, $L_\ell = L_s + L_r$. However, the following expressions can be employed in estimating a more accurate value for L_f.

$$L_f = B_m \frac{I_{inb}}{I_r} \tag{3.46}$$

where

$$B_m = \{(0.450\ V_{ic}/\omega_{ch}I_{inb})^2 + 2.78 \times 10^{-3}(1-\cos 2\phi_{eb})(|Z_{eb}|/\omega_{ib})^2\}^{0.5} \quad (3.47)$$

$$0.05 \leq I_r/I_{inb} < 0.1 \quad (3.48)$$

in which V_{ic} is the voltage of the power supply (Fig. 3.5), $\omega_c = 2\pi f_c$ being the chopping frequency of the chopper current source (Fig. 3.5), I_{inb} the inverter input current at the base speed, $\cos\phi_{eb}$ and $|Z_{eb}|/\omega_{ib}$ the values calculated in step (5) and I_r the rms of ripple current in the filter inductor L_f. Besides, the inductor should be rated for the following current and voltage:

$(I_f)_{max}$ = Maximum inductor current = $1.15\ I_{inb}$ (3.49)

$(V_f)_{max}$ = Maximum inductor voltage = $(\sqrt{3}\ E_1 + V_{ilc})$ or $(V_{ic}+V_{ilc})$ whichever is larger. The values of E_1 and V_{ilc} were given in step (5). (3.50)

(13) Estimate the maximum power loss in one thyristor, P_t, and in one diode, P_d, from the manufacturer's data sheet assuming a square-waveform current with a maximum current equal to I_{inb} and a maximum frequency equal to ω_{ip}. The total maximum loss in all thyristors and diodes are then,

$$P_{td} = 6(P_t + P_d) \quad (3.51)$$

(14) Estimate the total maximum power loss in the snubber resistances employing the following expressions:

$$P_{ts} = (9V_{ilc}^2 C_{tv} + 4.5\ V_{dm}^2\ C_{dv}) \cdot f_p \qquad (3.52)$$

$$V_{dm} \simeq 3\ I_{inb}\ \omega_o\ L_\ell \qquad (3.53)$$

$$f_p = \frac{\omega_{ip}}{2\pi} \qquad (3.54)$$

where V_{ilc} is the value determined in step (5), C_{tv}, C_{dv} are the thyristor and diode snubber capacitances found in steps (10) and (11), $L_\ell = L_s + L_r$ and ω_o was given in step (5).

(15) Calculate the inductor L_f maximum power loss from the following expression in which R_f is the inductor resistance,

$$P_f \simeq I_{inb}^2\ R_f \qquad (3.55)$$

(16) The approximate value of the maximum inverter power loss is obtained by adding the power losses estimated in steps (13), (14) and (15). In finalizing the inverter design, similar calculations to those mentioned in steps (13), (14) and (15) should be performed during one drive system duty cycle where the stator frequency, ω_i, and the inverter input current, I_{in}, may elect different values. The total inverter loss for a continuous drive system operation would then be attained by averaging the losses during one duty cycle. However, the inverter is designed such that, at the worst working conditions where the machine is delivering or accepting the maximum power at its peak shaft speed, no damage should arise during the permissible periods of such severe circumstances.

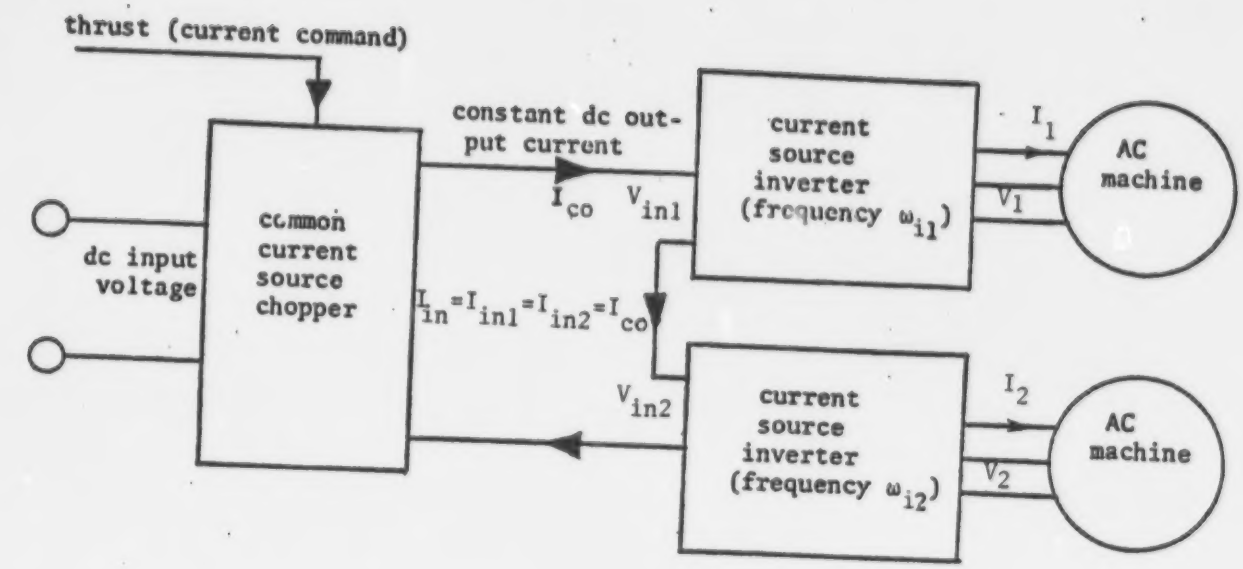
3.4.2 Inverter Design and Motor Selection for a Multi-Axle Drive System

The motor selection and the design procedure for the case of two inverters, connected either in series or in parallel, and supplied by a common chopper current source are quite similar to those of a single-axle drive. In the following, only those differences, requirements, and/or conditions which arise due to the utilization of two inverters in the drive system, are considered and defined. Regarding the requirements, the multi-axle traction drive systems have the following additional requirements:

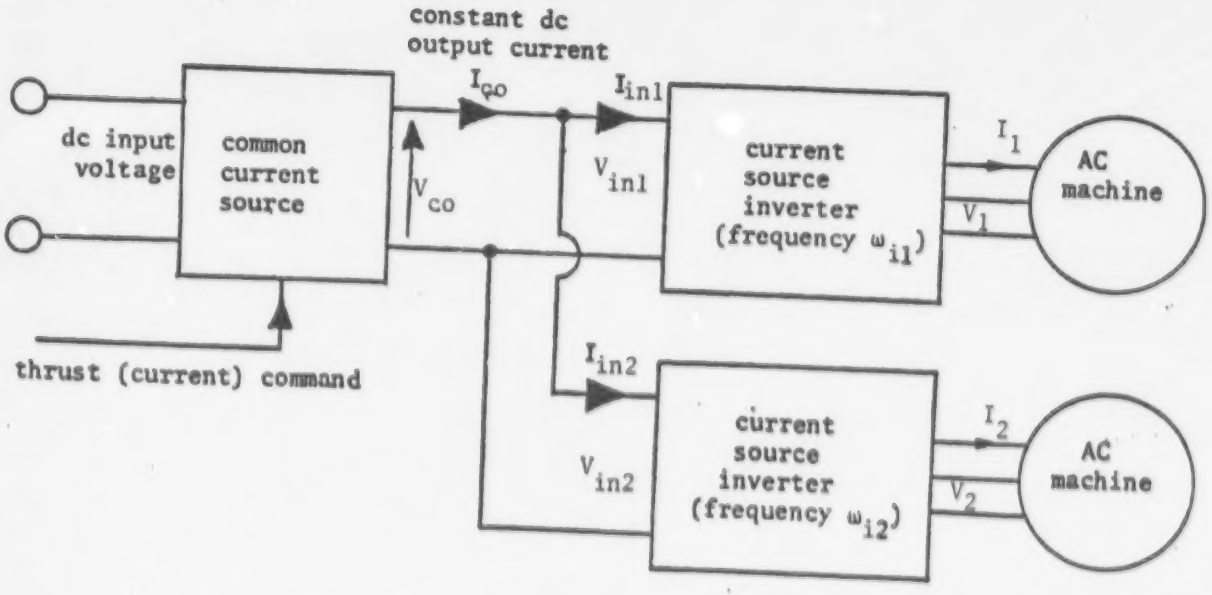
(1) In a multi-axle traction drive, the motors coupled to the individual drive axles operate at slightly different shaft speeds, due to small differences in the diameters of different wheel sets. An important drive system requirement is that the total torque be shared equally among the drive motors, independent of the differences in the shaft speeds.

(2) It is desirable that if the angular speed of an axle increases due to an excessive wear of the corresponding wheel set, then the torque transmitted through it (or the thrust at the wheel rim) be automatically reduced. This 'compensating' action tends to equalize the wear rate and keeps the wheel set diameters approximately equal during the operation of the traction drive.

The block diagram of Fig. 3.7 shows the series/parallel connections of two inverters to a common current source. Note that both inverter/motor sets have identical characteristics. For each connection the following can be observed.



a) Inverter stages connected in series.



b) Inverter stages connected in parallel.

Fig. 3.7 Block diagram of the series/parallel connections of two inverters to a common current source.

(a) Series Connections of Two Inverters

(1) The required torque at any speed for the drive system specified in Fig. 3.2 is equally supplied by the two machines. Each machine torque at base speed is:

$$\tau_{m1b} = \tau_{m2b} = \tau_{mb}/2 \tag{3.56}$$

(2) The inverter and motor input current at all speeds, including the base speed, are the same:

$$I_{in1b} = I_{in2b} = I_{inb} = I_{cob} = P_{mb}/V_{ic} \tag{3.57}$$

$$I_{1b} = I_{2b} = .78\ I_{in1b} = .78\ I_{in2b} = .78\ I_{inb} \tag{3.58}$$

(3) The shaft speed of each motor at base speed is given by,

$$\Omega_{m1b} = N_g v_b/r_1 \tag{3.59}$$

$$\Omega_{m2b} = N_g v_b/r_2 \tag{3.60}$$

where N_g is the gear reduction ratio, v_b the vehicle base speed, r_1 and r_2 are the radii of the wheels.

(4) The slip frequency of both the motors are the same so that the stator frequency of each machine at base speed is,

$$\omega_{i1b} = p\Omega_{m1b}/2 + \omega_{rb} \tag{3.61}$$

$$\omega_{i2b} = p\Omega_{m2b}/2 + \omega_{rb} \tag{3.62}$$

where p is the number of each machine poles. ω_{rb} is found in the same way as for a single motor drive

explained in step (9) of section 3.3.

(5) The thrusts F_{1b}, F_{2b} generated by each wheel at base speed are,

$$F_{1b} = N_g \tau_{m1b}/r_1 = N_g \tau_{mb}/2r_1 \qquad (3.63)$$

$$F_{2b} = N_g \tau_{m2b}/r_2 = N_g \tau_{mb}/2r_2 \qquad (3.64)$$

(6) The phase voltage and the power factor of each motor along with the input voltage of each inverter, all at the base speed, are calculated by using the following expressions:

$$R_{in1b} = \frac{R_r}{\omega_{rb}} \omega_{i1b} \frac{L_m^2}{(R_r/\omega_{rb})^2+(L_m+L_r)^2} \qquad (3.65)$$

$$X_{in1b} = \omega_{i1b} \left[L_s+L_m \frac{(R_r/\omega_{rb})^2+L_r(L_m+L_r)}{(R_r/\omega_{rb})^2+(L_m+L_r)^2}\right] \qquad (3.66)$$

$$Z_{in1b} = R_{in1b} + jX_{in1b} \qquad (3.67)$$

$$V_{1b}/\sqrt{3} = I_{1b} \cdot |Z_{in1b}| = .78\ I_{inb}|Z_{in1b}| \qquad (3.68)$$

$$\cos\phi_{in1b} = R_{in1b}/|Z_{in1b}| = \cos\phi_{inb} \qquad (3.69)$$

$$V_{in1b} = 1.35\ V_{1b} \cos\phi_{inb} \qquad (3.70)$$

$$R_{in2b} = \frac{R_r}{\omega_{rb}} \omega_{i2b} \frac{L_m^2}{(R_r/\omega_{rb})^2+(L_m+L_r)^2} \qquad (3.71)$$

$$X_{in2b} = \omega_{i2b} \left[L_s+L_m \frac{(R_r/\omega_{rb})^2+L_r(L_m+L_r)}{(R_r/\omega_{rb})^2+(L_m+L_r)^2}\right] \qquad (3.72)$$

$$Z_{in2b} = R_{in2b} + jX_{in2b} \tag{3.73}$$

$$V_{2b}/\sqrt{3} = I_{2b} |Z_{in2b}| = .78\ I_{inb} |Z_{in2b}| \tag{3.74}$$

$$\cos \phi_{in2b} = R_{in2b}/|Z_{in2b}| = \cos \phi_{inb} \tag{3.75}$$

$$V_{in2b} = 1.35\ V_{2b} \quad \cos \phi_{inb} \tag{3.77}$$

(7) The chopper current source output voltage is,

$$V_{cob} = V_{in1b} + V_{in2b} = 1.35\ \cos\phi_{inb} (V_{1b} + V_{2b}) \leq V_{ic} \tag{3.78}$$

(b) Parallel Connections of Two Inverters

(1) The chopper current source maximum output current is equal to the sum of the two inverter input currents at base speed,

$$I_{cob} = I_{in1b} + I_{in2b} = P_{mb}/V_{ic} \tag{3.79}$$

(2) The selection of the two induction motors is performed in the same way as for a single-motor drive, assuming the required power by the drive system at the base speed, to be shared equally by the two machines.

(3) The slip frequency, at the motoring mode, is the same for both the motors. The approximate value of the slip frequency at the base speed, ω_{rb}, is obtained in the same way as explained in step (9) of section 3.3 for a single-motor drive system whereas it is assumed that the required torque at base speed, τ_{mb}, is produced equally by the two induction machines.

(4) Obtain the shaft speed of each motor at base speed,

$$\Omega_{m1b} = N_g v_b / r_1 \tag{3.80}$$

$$\Omega_{m2b} = N_g v_b / r_2 \tag{3.81}$$

where N_g is the gear reduction ratio, v_b vehicle speed at the break point and r_1, r_2 the radii of the wheel sets.

(5) The stator frequency of each machine at the base speed is,

$$\omega_{i1b} = p\Omega_{m1b}/2 + \omega_{rb} \tag{3.82}$$

$$\omega_{i2b} = p\Omega_{m2b}/2 + \omega_{rb} \tag{3.83}$$

where p is the number of each machine poles and ω_{rb} was obtained in step (3).

(6) The input voltage of the two inverters at the base speed are the same and calculated by using the following expressions,

$$V_{cob} = 1.83\ I_{cob}(R_{in1b}R_{in2b})/(R_{in1b}+R_{in2b}) \leq V_{ic} \tag{3.84}$$

where I_{cob} was calculated in step (1) and R_{in1b}, R_{in2b} are respectively obtained by employing eqns. (3.65) and (3.71).

(7) The magnitudes of the line voltages of the two motors are the same and at base speed they are given by,

$$V_{1b} = V_{2b} = V_{cob}/(1.35 \cos \phi_{inb}) \tag{3.85}$$

in which V_{cob} was obtained in step (6) above and cos ϕ_{inb}

can be reckoned by using eqn. (3.69).

(8) The converter input currents at base speed are,

$$I_{in1b} = [R_{in2b}/(R_{in1b}+R_{in2b})]\ I_{cob} \qquad (3.86)$$

$$I_{in2b} = [R_{in1b}/(R_{in1b}+R_{in2b})]\ I_{cob} \qquad (3.87)$$

in which I_{cob} was given in step (1) and R_{in1b} and R_{in2b} are calculated by employing eqns. (3.65) and (3.71).

(9) The machine input currents and output torques at base speed are,

$$I_{1b} = .78\ I_{in1b} \qquad (3.88)$$

$$I_{2b} = .78\ I_{in2b} \qquad (3.89)$$

$$\tau_{m1b} = k_1\ I_{1b}^2 \qquad (3.90)$$

$$\tau_{m2b} = k_1\ I_{2b}^2 \qquad (3.91)$$

where

$$k_1 = \frac{3p}{2}\ \frac{R_r\ \omega_{rb}\ L_m^2}{[R_r^2+\omega_{rb}^2(L_r+L_m)^2} \qquad (3.92)$$

(10) The thrusts F_1 and F_2 appearing at each wheel rim are equal to

$$F_{1b} = N_g\tau_{m1b}/r_1 \qquad (3.63)$$

$$F_{2b} = N_g\tau_{m2b}/r_2 \qquad (3.64)$$

where N_g, r_1 and r_2 were defined in step (4).

(11) The ratio of the generated torques by the two machines at the base speed is,

$$\tau_{m1b}/\tau_{m2b} = (I_{1b}/I_{2b})^2 = (\omega_{i2b}/\omega_{i1b})^2 \quad (3.93)$$

And if the slip frequency, ω_{rb}, is small compared to the shaft speeds, Ω_{m1b} and Ω_{m2b}, we have,

$$\tau_{m1b}/\tau_{m2b} = (\omega_{i2b}/\omega_{i1b})^2 = [(1+d)/(1-d)]^2 \quad (3.94)$$

where d is the per unit differential wheel diameter and given by

$$d = (r_1 - r_2)/(r_1 + r_2) \quad (3.95)$$

(12) The per unit torque differential at base speed is obtained from,

$$\tau_{md} = (\tau_{m1b} - \tau_{m2b})/(\tau_{m1b} + \tau_{m2b}) = 2d(1+S_1)/(1+d^2+S_1^2+2S_1) \quad (3.96)$$

where

$$S_1 = \frac{\omega_{rb}}{\Omega_{m1b}}(1-d) \simeq \frac{\omega_{rb}}{\Omega_{m1b}} \quad \text{if } d << 1 \quad (3.97)$$

Also

$$\tau_{md} = 2d/(1+d^2) \quad \text{if } \omega_{rb}/\Omega_{m1b} << 1 \quad (3.98)$$

$$\tau_{md} = 2d \quad \text{if } d << 1 \quad (3.99)$$

(13) The ratio of F_{1b} and F_{2b} thursts and the per unit differential thurst are,

$$F_{1b}/F_{2b} = \left(\frac{\omega_{i2b}}{\omega_{i1b}}\right)^2 \left(\frac{1-d}{1+d}\right) \simeq \frac{1+d}{1-d} \quad (3.100)$$

$$F_d = (F_{1b} - F_{2b})/(F_{1b} + F_{2b}) \simeq d \quad (3.101)$$

(14) In the braking mode of operation, an unstable system results in if the slip frequencies of the two machines, whose driving inverters are in parallel, be kept equal to each other, $\omega_{r1} = \omega_{r2}$. In this case, a regulating current loop should be devised such that the difference of the two inverter input currents, $I_{in1} - I_{in2}$, at each operating point during regeneration, after being amplified by a gain equal to K, results in a slip perturbation, $\Delta\omega_r$, which should be added to and subtracted from the reference slip frequency of each motor, respe - tively. The following expressions specify the governing relationships and the value of gain K necessary for a stable system operation.

$$\begin{cases} \omega_{r1} = \omega_{ro} + \Delta\omega_r \\ \omega_{r2} = \omega_{ro} - \Delta\omega_r \end{cases} \tag{3.102}$$

$$\begin{cases} \omega_{i1} = \omega_{i10} + \Delta\omega_r \\ \omega_{i2} = \omega_{i20} - \Delta\omega_r \end{cases} \tag{3.103}$$

$$\begin{cases} \omega_{i10} = \Omega_{m1} + \omega_{ro} \\ \omega_{i20} = \Omega_{m2} + \omega_{ro} \end{cases} \tag{3.104}$$

$$\begin{cases} \Omega_{m1} = N_g v/r_1 \\ \Omega_{m2} = N_g v/r_2 \end{cases} \tag{3.105}$$

where ω_{ro}, ω_{i10} and ω_{i20} are respectively the slip frequencies and the stator frequencies of the machines

all at the desired operating point without any current regulation. Also v is the vehicle speed at any operating point. The slip frequency perturbation should be equal to:

$$\Delta\omega_r = K(I_{in1} - I_{in2}) = K(2I_{in1} - I_{co}) \qquad (3.106)$$

$$I_{co} = I_{in1} + I_{in2} \qquad (3.107)$$

$$K > - \frac{B_0(\omega_{i10}+\omega_{i20})}{2\, I_{co}(B_0+B_0'\omega_{i20})} \qquad (3.108)$$

where

$$B_0 = 1.83 \frac{R_r}{\omega_{r0}} \frac{L_m^2}{(R_r/\omega_{r0})^2+(L_m+L_r)^2} \qquad (3.109)$$

$$B_0' = 1.83\, R_r\, L_m^2 \frac{R_r^2-\omega_{r0}^2(L_m+L_r)^2}{[R_r^2+\omega_{r0}^2(L_m+L_r)]^2} \qquad (3.110)$$

If the differential wheel diameter is small,

$$\omega_{i10} = \omega_{i20} = \omega_{i0} \qquad (3.111)$$

Then

$$K > - \frac{\omega_{i0}}{I_{co}\left[1 + \frac{B_0'\omega_{i0}}{B_0}\right]} \qquad (3.112)$$

or

$$K > - \frac{\omega_{i0}}{I_{co}} \frac{1}{1+\left[\frac{R_r^2-\omega_{r0}^2(L_m+L_r)^2}{R_r^2+\omega_{r0}^2(L_m+L_r)^2}\right]\frac{\omega_{i0}}{\omega_{r0}}} \qquad (3.113)$$

in which if $R_r^2 >> \omega_r^2(L_m+L_r)^2$, then

$$K > -\frac{\omega_{i0}}{I_{co}} \frac{1}{1+\frac{\omega_{i0}}{\omega_{r0}}} \tag{3.114}$$

and if in eqn. (3.114), $\frac{\omega_{i0}}{\omega_{r0}} >> 1$, it yields

$$K > -\frac{\omega_{r0}}{I_{co}} \tag{3.115}$$

Note that in the regeneration mode $\omega_{r0} < 0$.

3.5 Design of Two Quadrant Chopper Current Source

The ac traction drive using the current source inverter (s) requires a 'current source' operating from a constant voltage dc input. The current source is a dc chopper whose output current is filtered by a series reactor and regulated by feedback. The chopper circuit provides a positive (unidirectional) output current at a positive or negative output voltage. The design procedure for the power circuit of a two quadrant chopper suitable for a regenerative ac drive using one or two current source inverters is outlined in the following. Fig. 3.8 shows the power circuit diagram of the chopper. The chopper output voltage is controlled by the constant frequency control strategy. Fig. 3.9 displays the block diagram of the chopper operation with regulation of its output current. The design steps are:

(1) Specify the chopping frequency, f_c , and calculate the chopping period,

$$T = 1/f_c \tag{3.116}$$

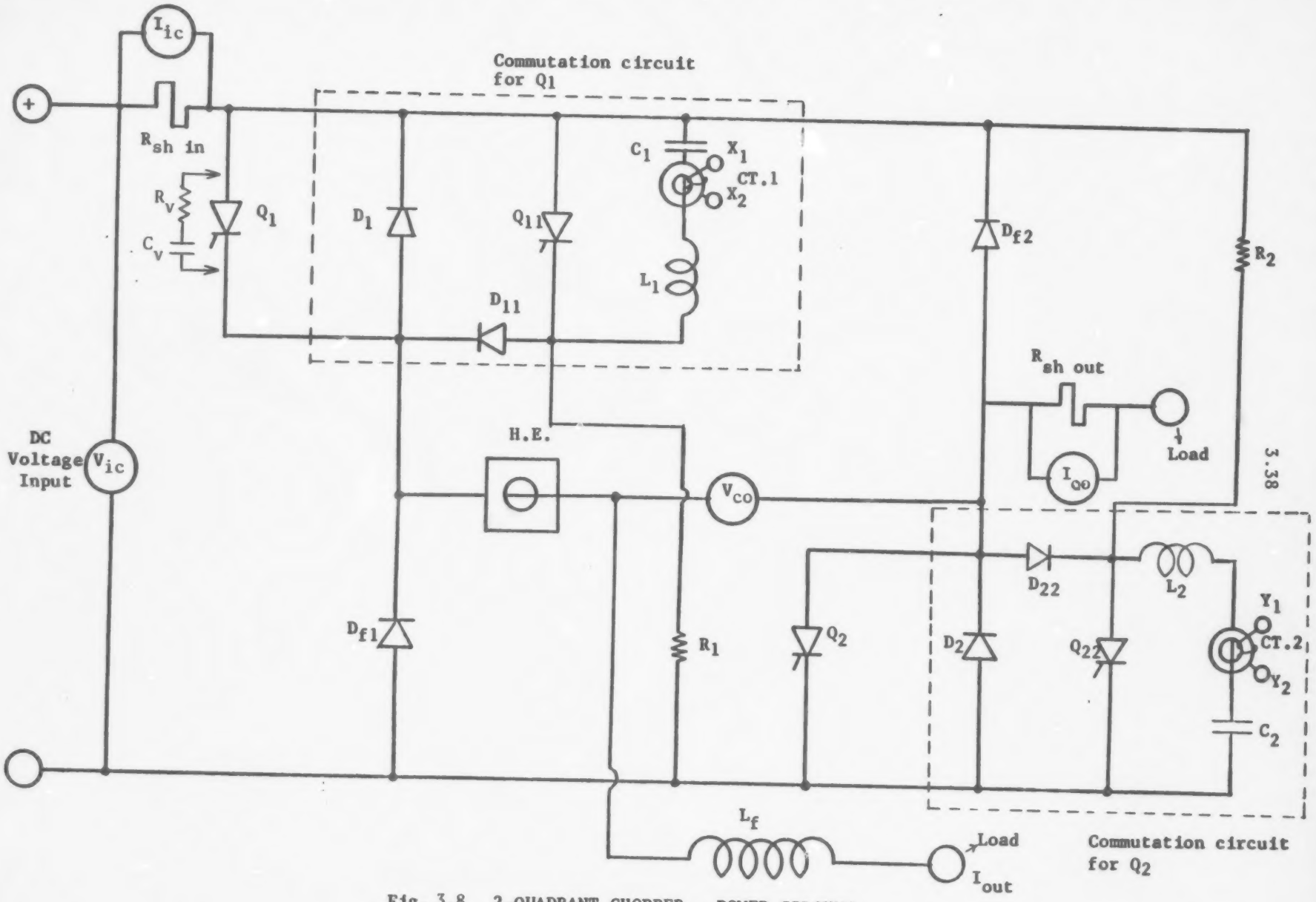


Fig. 3.8 2-QUADRANT CHOPPER - POWER CIRCUIT

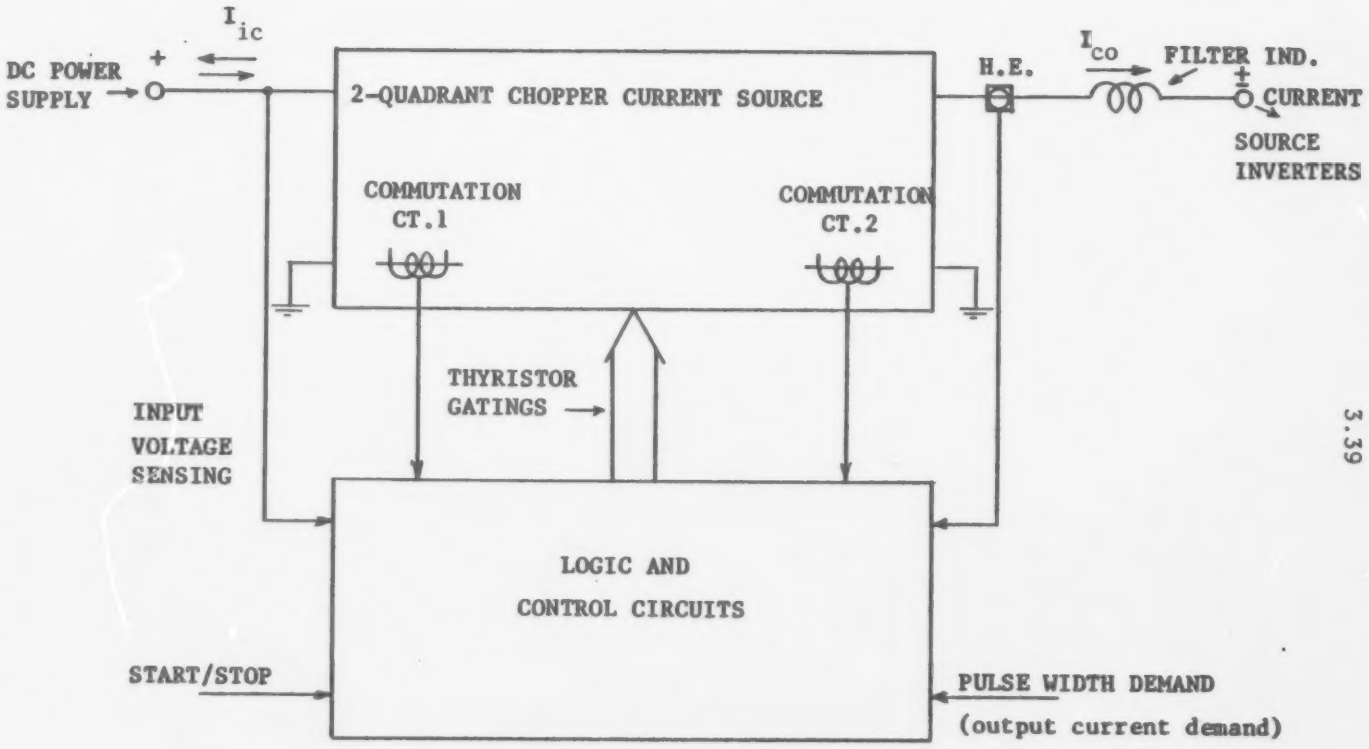


Fig. 3.9 Block diagram of the operation of the fixed frequency, 2-quadrant chopper current source of Fig. 3.8.

(2) The dc input voltage, V_{ic}, is the same as the value specified in Section 3.3.

(3) The maximum chopper output current is equal to the value of I_{cob} determined by eqn. (3.57) or (3.79) in Section 3.4.

(4) The value of the commutation inductance $L_1=L_2$ is given by the following expression,

$$L_1 = L_2 = \frac{t_q}{\pi - 2\sin^{-1}(1/X)} \cdot \frac{V_{ic}}{XI_{cob}} e^{-.75\pi/Q} \qquad (3.117)$$

where t_q is the turn-off time provided by the commutation circuit and chosen to be between 25-100 μs, Q the quality factor of L_1 selected to be between 5-20 and X a design parameter considered to be between 2-4.

The peak voltage and current of the inductors L_1 and L_2 are,

$$V_{\ell p} = V_{ic} \qquad (3.118)$$

$$I_{\ell p} = XI_{cob} \qquad (3.119)$$

The maximum rms current in L_1 and L_2 is given by

$$I_{\ell r} = \frac{\sqrt{2}}{2} I_{cob} X(2\pi\sqrt{L_1C_1}/T)^{\frac{1}{2}} \qquad (3.120)$$

in which C_1 is given in the next step and T was given in step (1) above.

(5) The size of the commutation capacitor $C_1=C_2$ is calculated from,

$$C_1 = C_2 = \frac{t_q}{\pi - 2\sin^{-1}(1/X)} \frac{XI_{cob}}{V_{ic}} e^{.75\pi/Q} \quad F \tag{3.121}$$

where t_q, X and Q are the same as the values given in the previous step.

The capacitor peak voltage, peak and maximum rms currents are:

$$V_{cp} = V_{ic}(1 + 1/X) \tag{3.122}$$

$$I_{cp} = X\ I_{cob} \tag{3.123}$$

$$I_{cr} = \frac{\sqrt{2}}{2}\ I_{cob} X (2\pi\sqrt{L_1 C_1}/T)^{\frac{1}{2}} \tag{3.124}$$

(6) The ratings of the auxiliary thyristors Q_{11} and Q_{22} are:

$$V_{cct} = V_{ic}(1 + 1/X) \tag{3.125}$$

$$I_{t'p} = \text{peak current} = I_{cob} X\ e^{\pi/2Q} \tag{3.126}$$

$$I_{t'r} = \text{rms current} = \frac{\sqrt{2}}{2}\ I_{cob} X\ e^{\pi/2Q} (\pi\sqrt{L_1 C_1}/T)^{\frac{1}{2}} \tag{3.127}$$

(7) The ratings of the series diodes D_{11} and D_{22} are:

$$V_{d'} = \text{Peak reverse voltage} = V_{ic}(1 + 1/X) \tag{3.128}$$

$$I_{d'p} = \text{Peak current} = I_{cob} X \tag{3.129}$$

$$I_{d'r} = \text{rms current} = \frac{\sqrt{2}}{2}\ I_{cob} X (\pi\sqrt{L_1 C_1}/T)^{\frac{1}{2}} \tag{3.130}$$

(8) The ratings of the feedback diodes D_1 and D_2 are:

$$V_{d''} = \text{Peak reverse voltage} = V_{ic}(1 + 1/2X) \tag{3.131}$$

$$I_{d''p} = \text{Peak current} = I_{cob}X \tag{3.132}$$

$$I_{d''r} = \text{rms current} = \frac{\sqrt{2}}{2} I_{cob}X(\pi\sqrt{L_1C_1}/T)^{\frac{1}{2}} \tag{3.133}$$

(9) The values of the discharge resistors R_1 and R_2 are chosen to be,

$$R_1 = R_2 = 2T/3C_1 \tag{3.134}$$

(10) The current ratings of the main thyristors Q_1, Q_2 in Fig. 3.7 are,

$$I_{tr} = \text{Thyristor rms current} = I_{cob}\sqrt{D_t} \tag{3.135}$$

$$I_{ta} = \text{Thyristor average current} = I_{cob}D_t \tag{3.136}$$

where D_t is the duty cycle of the thyristors which is a function of the operating conditions of the drive and given by,

$$D_t \simeq \frac{1}{2T}\left[T \pm T_{on} + \frac{\pi+\theta_1}{\omega}\right] \tag{3.137}$$

where the plus sign is applicable to a positive output voltage and minus sign to a negative output voltage. Also, T is the chopping period determined in step (1) above, T_{on} is the width of the chopper output voltage pulse during each chopping period, θ_1 and ω are quantities obtained from,

$$\omega = \omega_0 \sqrt{1 - 1/(4Q^2)} \tag{3.138}$$

$$\omega_0 = 1/\sqrt{L_1 C_1} \tag{3.139}$$

$$\sin \theta_1 = \frac{I_{cob}\, \omega L_1}{V_{ic}}\, e^{\frac{\omega_0}{\omega}\frac{1}{2Q}(\pi+\theta_1)} \tag{3.140}$$

where L_1 and C_1 were determined in steps (4) and (5) and Q being the quality factor of L_1. The exact value of Q can be decided after the selection of L_1. Note that eqn. (3.140) is solved numerically. In the event of a large Q it follows,

$$\omega \simeq \omega_0 \tag{3.141}$$

$$\theta_1 = \sin^{-1}\left[\frac{I_{cob}}{V_{ic}}\ \frac{L_1}{C_1}\, e^{(\pi+\theta_1)/2Q}\right] \tag{3.142}$$

In addition, eqn. (3.137) can be written in the following simpler form if the commutation interval is small.

$$D_t \simeq \frac{1}{2T}\,[T \pm T_{on}] \tag{3.143}$$

The voltage rating of the main thyristors is,

$$V_{cmt} = V_{ic}\left(1 + \frac{1}{2X}\right) \tag{3.144}$$

where X is a design factor chosen between 2 and 4.

The main thyristors available turn-off time, t_q, which was selected between 25-100 μs in step (4), can be calculated at this point to be,

$$t_q \simeq \sqrt{L_1 C_1}\ (\pi - 2\theta_1) \tag{3.145}$$

The selection of the main thyristors, Q_1, Q_2, depends upon the total power loss during the duty cycle of the drive. The power loss can be calculated at each value of T_{on} from the manufacturer's data sheet corresponding to duty cycle D_t. The total power loss can be determined by repeating the calculations over the profile of T_{on} at different operating speeds.

(11) Calculate the size of the protective inductor in series with one of the chopper input terminals (not shown in Fig. 3.7),

$$L_\ell \geq V_{ic}/(di/dt)_{max} \qquad (3.146)$$

where $(di/dt)_{max}$ is the maximum allowable rate of rise of the anode current.

(12) The current ratings of the freewheeling diodes, D_{f1}, and D_{f2} in Fig. 3.7, are,

$$I_{dr} = \text{Diode rms current} = I_{cob}\sqrt{D_d} \qquad (3.147)$$

$$I_{dr} = \text{Diode average current} = I_{cob}\, D_d \qquad (3.148)$$

where D_d is the duty cycle of the diodes and given in the following for the case that the commutation interval is small,

$$D_d \simeq \frac{1}{2T}\,(T \mp T_{on}) \qquad (3.149)$$

In the above equation the minus sign is applicable to a positive output voltage and the plus sign to a negative output voltage.

The diode peak reverse voltage is,

$$V_d = V_{ic} \tag{3.150}$$

The selection of the freewheeling diodes is conducted in a similar way as mentioned in step (10) for the main thyristors. The total power loss in the diodes over the duty cycle of the drive can be obtained by calculating the loss at each value of T_{on}.

(13) Select the values of snubber, resistance, R_v, and capacitance, C_v, such that

$$C_v = 0.1 - 0.2 \quad F \tag{3.151}$$

$$R_v = 2\sqrt{3L_\ell/C_v} \tag{3.152}$$

where L_ℓ is the di/dt inductance in series with the chopper input terminal and given in step (11) above. The maximum value of the rate of rise of the forward voltage across the thyristors can be checked by employing the following equations:

$$(dv/dt)_{max} = V_{c12}\,\frac{R_v}{3L_1} \tag{3.153}$$

where

$$V_{c12} \simeq V_{ic}\, e^{-(2\pi-\theta_1)2Q}\,(\cos\theta_1 - \frac{1}{2Q}\sin\theta_1) \tag{3.154}$$

In the above equation, Q is the quality factor of the commutation inductance, L_1, and θ_1 was given in step (10) above.

(14) The total power loss in the main thyristors and in the freewheeling diodes is obtained by adding the losses calculated in steps (10) and (11).

(15) Calculate the power loss in the auxiliary thyristors Q_{11} and Q_{22} from the manufacturer's data sheet for a sinusoidal pulse of duration $\pi\sqrt{L_1C_1}$ and a peak current of $I_{cob}\, e^{\pi/2Q}$.

(16) The power loss in the commutation circuits is estimated from the following expressions:

$$P_c = \frac{1}{2} C_1 V_{ic}^2 \left[A + \frac{f_c}{f_0} B + \frac{L_\ell}{L_1} D + 4.5 \frac{C_v}{C_1} \right] f_c \qquad (3.155)$$

where

f_c = chopping frequency given in step (1)

$$f_0 = 1/2\pi\sqrt{L_1C_1} \qquad (3.156)$$

$$A = 1 - \left\{ \exp[-(2\pi - \sin^{-1}\tfrac{1}{X})/Q] \left(1 - \frac{1}{X^2}\right) \right\} + \frac{\pi}{2QX^2} \exp(1.5\pi/Q) \qquad (3.157)$$

$$B = \frac{q}{\pi} \left\{ 2\pi + [1 - \exp(-2\pi/Q)] \frac{Q}{2} \right\} \qquad (3.158)$$

$$D = \exp(-1.5\pi/Q)/X^2 \qquad (3.159)$$

$$q = T_c/(R_1C_1) = 2.5 - 4 \qquad (3.160)$$

in which T_c is the duration of each commutation process.

CHAPTER 4

CONCLUSIONS

4. CONCLUSIONS

This final report concludes the project on research and development of ac squirrel-cage induction motor driven propulsion systems. Earlier reports have shown that from the different options of available ac drives in terms of ac machine types, the method of conversion of a constant dc voltage to a variable-frequency ac supply and the control strategy, there exists a preferred system best suited for most traction applications. Such a system consists of a fixed-frequency chopper current source, one or two (in series or parallel) current source inverters and one or two squirrel-cage induction machines with slip-frequency control strategy. The advantages of this selected system over the other options are ruggedness, simplicity of design and operation, decrease of ripples in input current, regeneration and no system derating with a large difference in wheel diameters.

The feasibility of operation of systems with higher power levels than those observed in earlier studies has been demonstrated by performing tests on a 125/250 kW, one-/two-motor, experimental drive system. The results of these tests have also been employed to verify and/or modify the design procedures outlined in the earlier reports, thus establishing the final step-by-step basic design procedure for each unit. The tests have covered both steady-state and dynamic operations in motoring and braking regions. All the tests have been conducted at operating points located on a typical traction torque/speed curve consisted of three modes of operation: (a) constant torque, (b) constant power and (c) cruising.

The conducted tests along with the investigations reported in the earlier phases of this project have established a solid base for basic design procedures for single- and multi-axle traction drive systems similar to the experimental unit. These design steps have been the direct consequence of the good agreement between the theoretical predictions and the experimental results of this study. These design steps can provide a good starting point in designing a specific drive system for any transportation applications like trolly coaches, subway cars, etc. This design can further be modified in the stage of circuit set-up where the accurate measurements, especially those of losses, determine the final selection of the components.

The block diagram of the preferred ac traction drive system with two inverters in parallel along with a brief description of the function of each component/unit have been given in Chapter I of this report. The different units of the experimental drive system have also been identified by presenting a block diagram in the same chapter. The details of the circuit and the operation of these units have been covered in four appendices in this report. Chapter I has been concluded by discussing the design features of the experimental drive system and specifying the advantages of a fixed-frequency chopper current source over the one with a frequency-modulation control strategy. Chapter II of this report has established the objectives of performing the tests with typical traction drive torque and power profiles. Some of the parameters to be measured during the tests have been specified on a block diagram of the experimental drive following which the function and the characteristics of each unit have been explained. The details

of the performed tests along with the parameters to be measured on each unit have also been provided in Chapter II. Chapter III of this report has been assigned to detailed descriptions of the characteristics of different units in a traction drive system and the corresponding design procedures. For a monomotor traction drive system, the selection of the squirrel-cage induction motor and the design of the current source inverter have been given in a simplified, step-by-step method. For a two-motor traction drive system two cases have been dealt with; one in which the two inverters are in series and the other where they are in parallel. For these two cases, the selection of the induction motors and the design of the inverters are almost similar to those for a mono-motor system so that only the steps different from the former have been described. It has been concluded that for a series connection of the inverters and for either a motoring or braking mode of operation the vehicle demanded torque is contributed equally by both drive motors thus requiring the same slip frequency for the two machines. However, in a parallel connection of the two inverters the slip frequencies can be adjusted equal to each other only in a motoring mode of operation. In a braking mode of operation, it has been observed that the two slip frequencies should be different if a stable system is desired. In this case, a regulating slip frequency loop is employed such that the difference of the two inverter currents at each operating point, after amplification, results in a slip perturbation which is added to the reference slip frequency of the drive motor with a higher input current and subtracted from the reference slip frequency of the drive motor with a lower input current. The

design of the chopper current source has also been covered in Chapter III where it is applicable both to a mono- and a two-motor traction drive system.

Future basic work should be carried out in the application of permanent magnet synchronous motors in propulsion systems. Due to the lack of an externally-excited rotor, these machines represent a robust construction along with a better efficiency and higher speeds compared with the induction-type machines. In practice, however, to utilize these advantages, a permanent magnet synchronous machine requires a power conditioner capable of producing a defined output voltage or current waveform. Under these circumstances, the shaft position angle, δ, must be controllable on a cycle by cycle basis. In addition, due to the self-commutation characteristics of the inverter with a permanent magnet synchronous motor load, we should be able to improve the power conditioner design in terms of its simplicity, efficiency, size and cost. With the continuing improvements in the transistor, thyristor and microprocessor technologies and also in the quality of permanent magnets, the new generation of ac traction drive systems are likely to employ permanent magnet synchronous machines as the main drive motor.

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Traction System Specifications

Toronto Transit Commission
Canadian National Railways
Canadian Pacific Railways
Transportation Development Centre

APPENDIX A

DC POWER SUPPLY UNIT

APPENDIX A

DC POWER SUPPLY UNIT

A1 Introduction

The dc power required for supplying the chopper unit in the test system is provided by a dc power supply unit capable of operating with a unidirectional output voltage and a bidirectional current. The only power supplied by the ac source feeding this dc power supply unit is consumed as losses in the whole test system. In the following the specifications and the detailed description of a dc power supply unit fulfilling the above requirements are given and all its features discussed.

A2. Specifications

Fig. A1 displays the block diagram of the required dc power supply unit. This block diagram is equivalent to transformer, "p" controlled rectifier, "N" controlled rectifier and filter, blocks shown in Fig. 1.1. The dc power supply unit is capable of supplying or accepting 240 KW of power at a nominal 600 VDC voltage and a nominal 400 ADC current. This unit provides the necessary power for driving two 125-HP motors in the test system both in motoring and braking regions. However, a propulsion system up to 400-HP can also be tested with this unit. The specifications of the different parts of the dc power supply unit of Fig. A1 is given in Table A1. The detailed descriptions of these parts are covered in the next section.

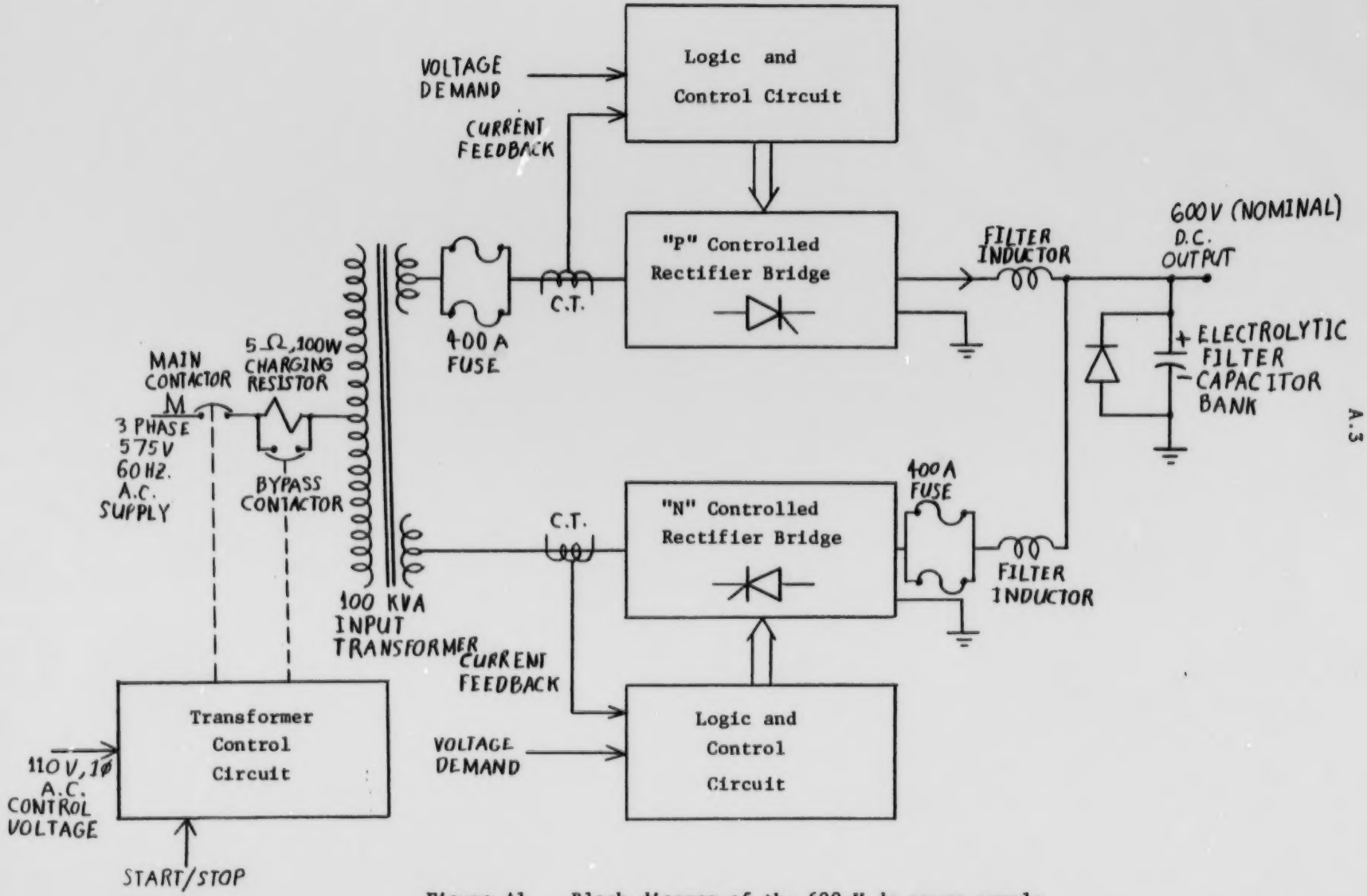


Figure A1 Block diagram of the 600 V dc power supply

Part of Unit	Specifications
Transformer	Primary: 3-ph., 60 Hz , 100 KVA, 575V ± 30% (with 5 taps), air-cooled. Secondaries (two isolated windings each consisting of 4 coils which can be conected in series or parallel), each: 3-phase, 60 Hz , 400 KVA, 460V, water-cooled.
"P" Controlled rectifier	Input: Connected to secondary winding #1, clamped. Output: 400-800 VDC (across filter capacitor) 0-400 ADC (with filter reactor), 0<delay angle (β_1)<90 °, 240KW. Cooling: Air.
"N" Controlled rectifier	Input: Connected to the filter capacitor, 400-800 VDC, 0-400 ADC, 240 KW, 90 ° < delay angle (β_2) < 180 ° Output: Connected to secondary winding #2, clamped. Cooling: Air.

Table A1 Specifications of transformer, "P" and "N" controlled rectifiers of the dc power supply unit.

A3 DETAILED SYSTEM DESCRIPTION

A 240 KW power supply system based on the specifications given in section A2 is described in this section. The basic block diagram of the 600V dc power supply was shown in Figure A1. The general function of different blocks in this figure along with a detailed description of each one is presented in the following.

The system is supplied from a three-phase, 575V, 60Hz ac supply, which is connected to an input transformer. The transformer has two independent secondary windings which feed two controlled rectifier bridges. The provision of independent secondary windings eliminates the need for a large interphase reactor to limit the circulating current. The positive controlled rectifier bridge provides path for current flowing from the supply to the load. The input ac lines of the positive bridge are protected by 400 A fuses. A logic and control unit with an outer voltage feedback loop and an inner current loop controls the firing angle of the thyristors in the positive (P) bridge. The thyristors are cooled by forced air circulation.

The negative (N) controlled rectifier bridge provides path for the current flowing from the load to the ac supply, during regeneration. The load lines are protected by a 400 A fuse for a fault in the bridge. The negative bridge is controlled by a logic and control circuit which is similar to the positive bridge.

The output terminals of the controlled rectifier bridges are connected in parallel through series filter reactors (Figure A.1). The filter reactors provide the impedance to limit the ripple current in the two bridges. An electrolytic filter capacitor bank with a reverse diode is connected at the output terminals to provide a ripple free dc output voltage.

The following blocks in Figure A1 are described in detail in the following:

(1) Transformer Control Circuit

(2) Input Transformer

(3) Controlled Recrifier Bridge (Positive)

(4) Controlled Rectifier Bridge (Negative)

(5) Logic and Control Circuit.

A 3.1 Transformer Control Circuit

The 575 V, 3-phase, 60 Hz, ac input is connected to the transformer through a main contactor M (Figure A1) and a 5 ohm, 100 W charging resistor. The charging resistors limit the inrush current of the input transformer when the main contactor is closed. A second contactor is used to bypass the charging resistors after a suitable delay.

Figure A2 shows the 'transformer control circuit' of Figure A1 in detail. A control voltage of 110 V ac is applied to the starting contactor S when the START button is pressed. This closes contacts S_1 and S_2 and energizes the main contactor M. The 575 V ac power is then applied to the input transformer through the 5 ohm charging resistors.

When contacts S_1 and S_2 close, the 110 V control voltage starts charging an R-C network through the rectifier. After a delay, the auxiliary contactor A is energized, closing contact A_1 and energizing the bypass contactor B. Therefore, after a delay determined by the R-C network, the charging resistors are bypassed and the 575 V input power is directly connected to the primary windings of the input transformer.

When contacts S_1 and S_2 are closed the indicator light is turned on and the alarm bell is isolated from the 110 V control voltage, if the water flow switch is open. If the flow of transformer cooling water is interrupted, the water flow switch is closed and the alarm is actuated.

When the STOP button (Figure A2) is pressed the supply to the starting contactor S is interrupted and the main contactor M is opened. After a small delay, the bypass contactor is also opened.

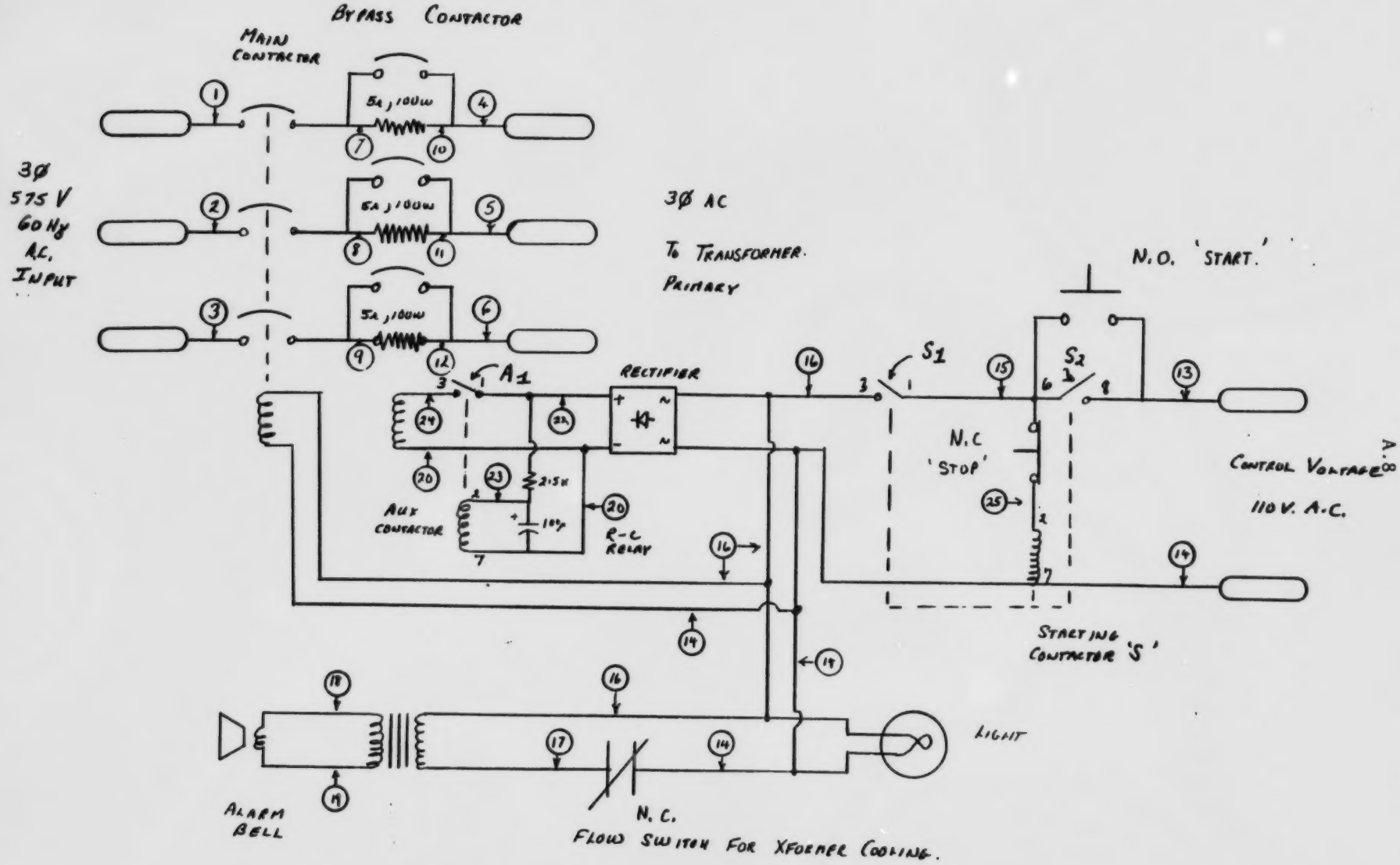


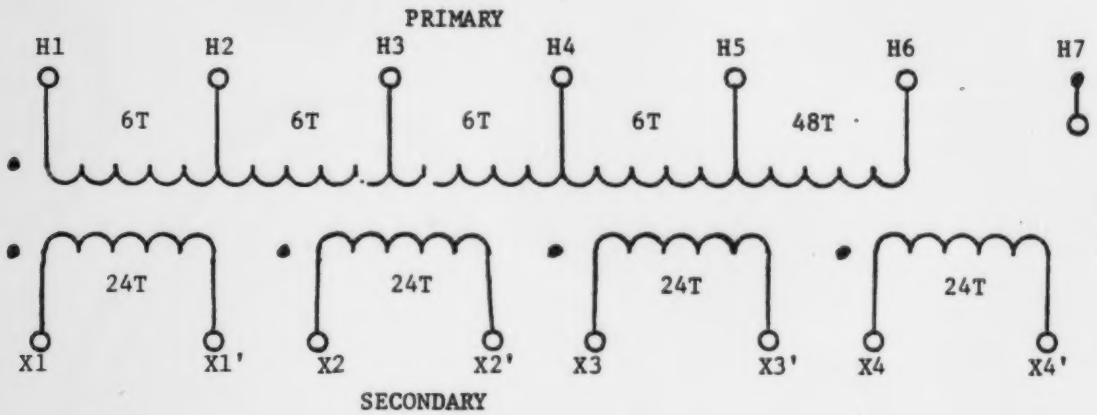
Figure A.2 TRANSFORMER CONTROL CIRCUIT showing main contactor M, 5Ω charging resistors, start/stop and alarm circuits.

A.3.2 Input Transformer

The input transformer provides isolated ac supplies to the two controlled rectifier bridges. The nominal voltage ratio is 575 V (Primary)/460 V (each secondary). However, the primary winding is provided with 5 taps and the secondary winding consists of 4 coils which can be connected in series or parallel. Figure A3 shows the single leg winding configuration and the range of secondary voltages with different connections. The provision of different taps provides the versatility of performing system tests at different secondary voltages. This is particularly useful in testing the system modules as the input voltage can be increased in steps from a low value.

The input transformer has water cooled secondary windings, each rated at 400 KVA. Each secondary winding with two series connected coils provides the 575/460 V ratio as underlined in Figure A 3. The provision of independent secondary windings for each bridge enables the bridges to operate independently with positive and negative load current or together with a small circulating current. The transformer is isolated by fuses (Figure A1 .) if there is a short circuit on the secondary side due to a fault in the rectifier bridges. The loss of cooling water in the secondary windings triggers an alarm (Figure A 2).

SINGLE LEG WINDING CONFIGURATION



PRIMARY (575 V_{ac}, 60 Hz)	SECONDARY	VOLTAGE RANGE WITH PRIMARY TAP H1	H2	H3	H4	H5
Y	SINGLE COIL Y	191	209	230	256	288
	" " Δ	110	120	133	147	166
	DOUBLE " Y	383	418	460	511	575
	" " Δ	221	241	266	295	332
	TRIPLE " Y	575	627	690	767	862
	" " Δ	331	361	399	442	498
	QUAD " Y	767	836	920	1022	1150
	" " Δ	442	482	532	590	664
Δ	SINGLE COIL Y	332	362	398		
	" " Δ	191	209	230		
	DOUBLE " Y	664	724	797		
	" " Δ	383	418	460		
	TRIPLE " Y	996	1086	1195		
	" " Δ	574	627	690		
	QUAD " Y	1328	1449	1593		
	" " Δ	766	836	920		

- PRIMARY DELTA MINIMUM NUMBER OF TURNS AT 575 V_{ac} IS 60.

Figure A 3 The winding arrangement and range of secondary voltages of the 400 KVA input transformers.

A3.3 "P" Controlled Rectifier Bridge

The 460 V, 3-phase, ac power from the secondary winding of the transformer is converted to 600 V (nominal) dc output by a three-phase controlled rectifier bridge. An L_f-C_f filter is connected at the output of the bridge to filter the ripple in the output voltage.

Figure A4 shows the power circuit diagram of the "P" controlled rectifier bridge. The input lines of the bridge are protected by 400A fuses. The secondary windings of the current transformer (C.T.) are connected in star and the rectified output signal is proportional to the dc output current of the bridge. Each of the thyristors Q_1 to Q_6 of the bridge are protected against di/dt and commutation dv/dt by the series inductors L_s and snubber network R_v, C_v. The output filter capacitor bank, C_f, is of the electrolytic type and is provided with the discharge resistors R_f and clamping diode D_f. Diode D_f prevents the reversal of polarity on the capacitors C_f. A 'peak clamping circuit' is provided at the ac input terminals of the bridge to clamp the reverse voltage spikes on the thyristors during commutation. The clamping circuit also absorbs the transient voltage spikes which may be present on the ac input lines.

Table A2 gives the specifications of the components of the "P" controlled rectifier bridge of Figure A.4. Figures A5 shows the power circuit diagram of Figure A4 in detail. The connections between the components of the bridge are identified by numbers which can be traced on the unit. Figure A6 and A7 provide the connection diagrams of the 'peak voltage clamping' and the 'current feedback rectifier' circuits respectively.

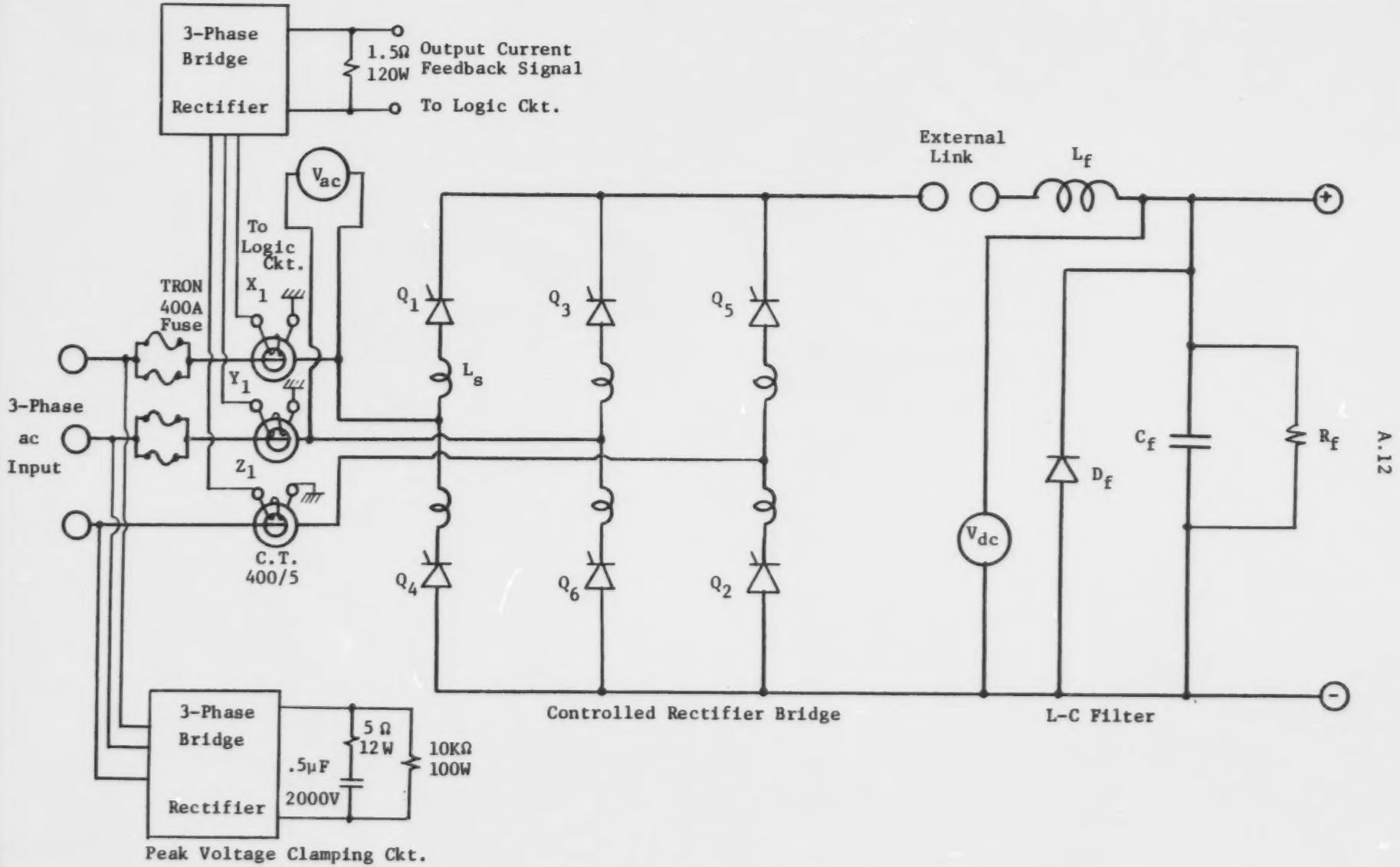


Figure A.4 Power circuit diagram of the "P" (positive) controlled rectifier bridge.

Table A2

Specifications of the components of "P" controlled rectifier bridge.

S.N.	Component	Specifications
1	Thyristor (Q_1 to Q_6)	GE C448PB, 725 A (rms), 300 V, t_q= 40 μs.
2	Current Transformer (C.T.)	Westinghouse type 145P667H01 400:5
3	Series Inductors, L_s	7 μH, 350 A
4	Snubber Networks, R_v C_v	10Ω, 50W Non-inductive ohmile 0.2 μF, 1000V, WIHA Capacitors
5	Filter Inductor, L_f	2.0 mH, 400A, 2 in series of 45 turns, 14" diameter
6	Filter Capacitor, C_f	12 x 4000 μF, 350 V, Computamile FAHM 4000-350 D6
7	Discharge Resistor, R_f	500Ω, 200W ohmile 1361
8	Clamping Diode, D_f	GEA96P

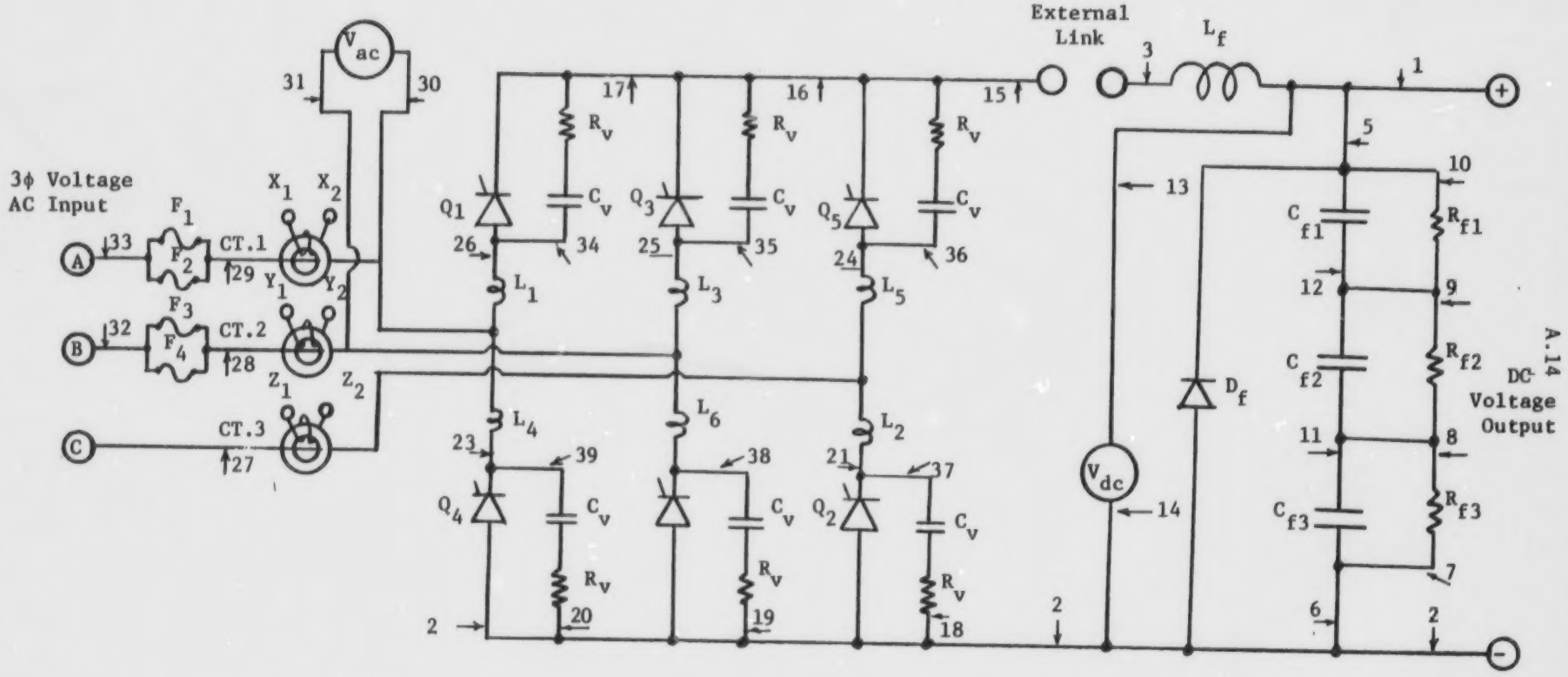


Figure A5 POSITIVE BRIDGE - DETAILED POWER CIRCUIT
The numbers indicate the wire connections between the different components of the bridge. External link may be used for connecting extra inductance in series with L_f.

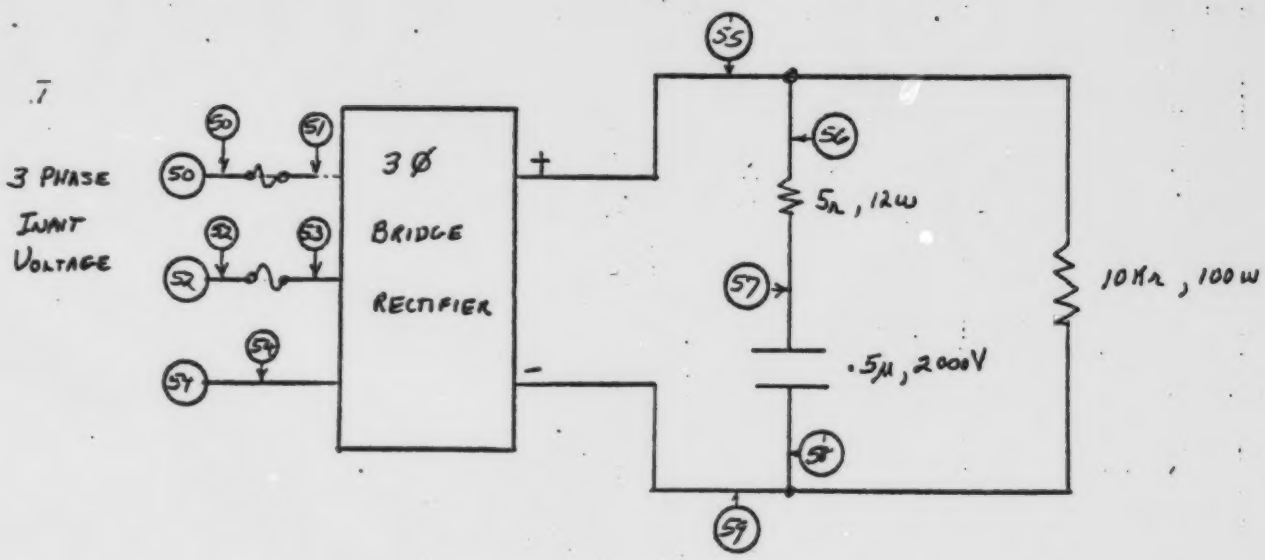


Figure A6 PEAK VOLTAGE CLAMPING - RECTIFIER UNIT

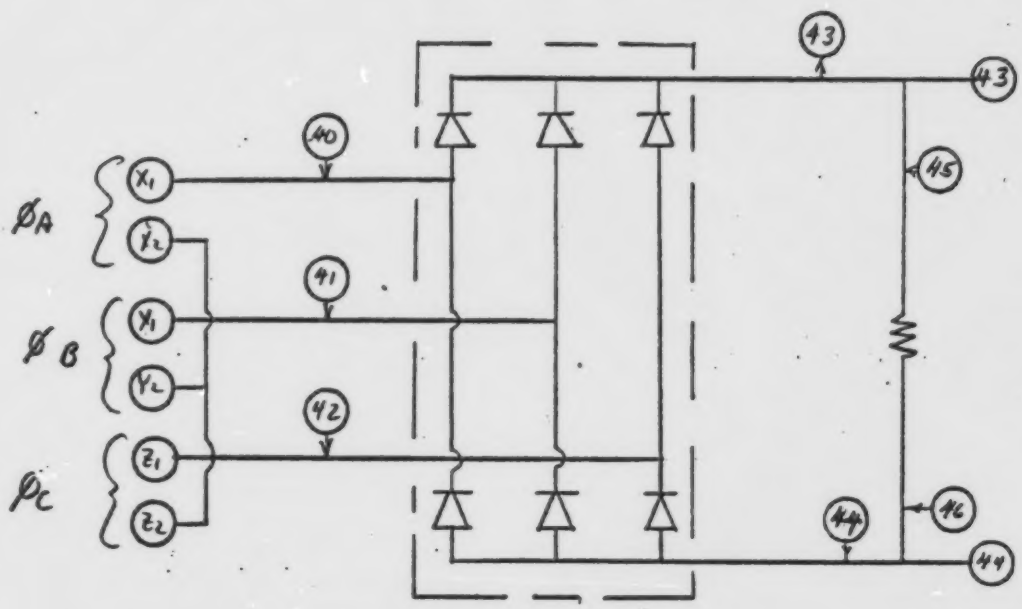


Figure A7 CURRENT FEEDBACK - RECTIFIER UNIT

A3.4 "N" Clamping Controlled Rectifier Bridge

The "N" controlled rectifier bridge is connected to receive negative dc output current from the load. It therefore converts dc power from the output (load) terminals to the ac power at the three phase input. A filter inductor L_f is connected in series with the bridge to filter the dc current.

Figure A8 shows the power circuit diagram of the "N" controlled rectifier bridge. The circuit is similar to the positive bridge except that the fuses are connected in the dc line to isolate the bridge in the event of a failure. A contactor is connected in series with the ac input lines, to provide sequencing of the logic and power circuits during starting. The output of the "P" and "N" controlled rectifier bridges are connected in parallel as shown in Figure A1 . Therefore, the output voltage polarity of the negative bridge is as shown in Figure A8 and it is operated with a phase angle greater than $\pi/2$ (inverter operation).

Figure A9 shows the power circuit diagram of the bridge in detail. The connections between different components have been identified by numbers which can be traced on the unit. Similarly, Figures A10 and A11 give the connection diagrams of the 'peak voltage clamping' and the 'current feedback' circuit respectively. Table A3 shows the specifications of the different components of the "N" bridge.

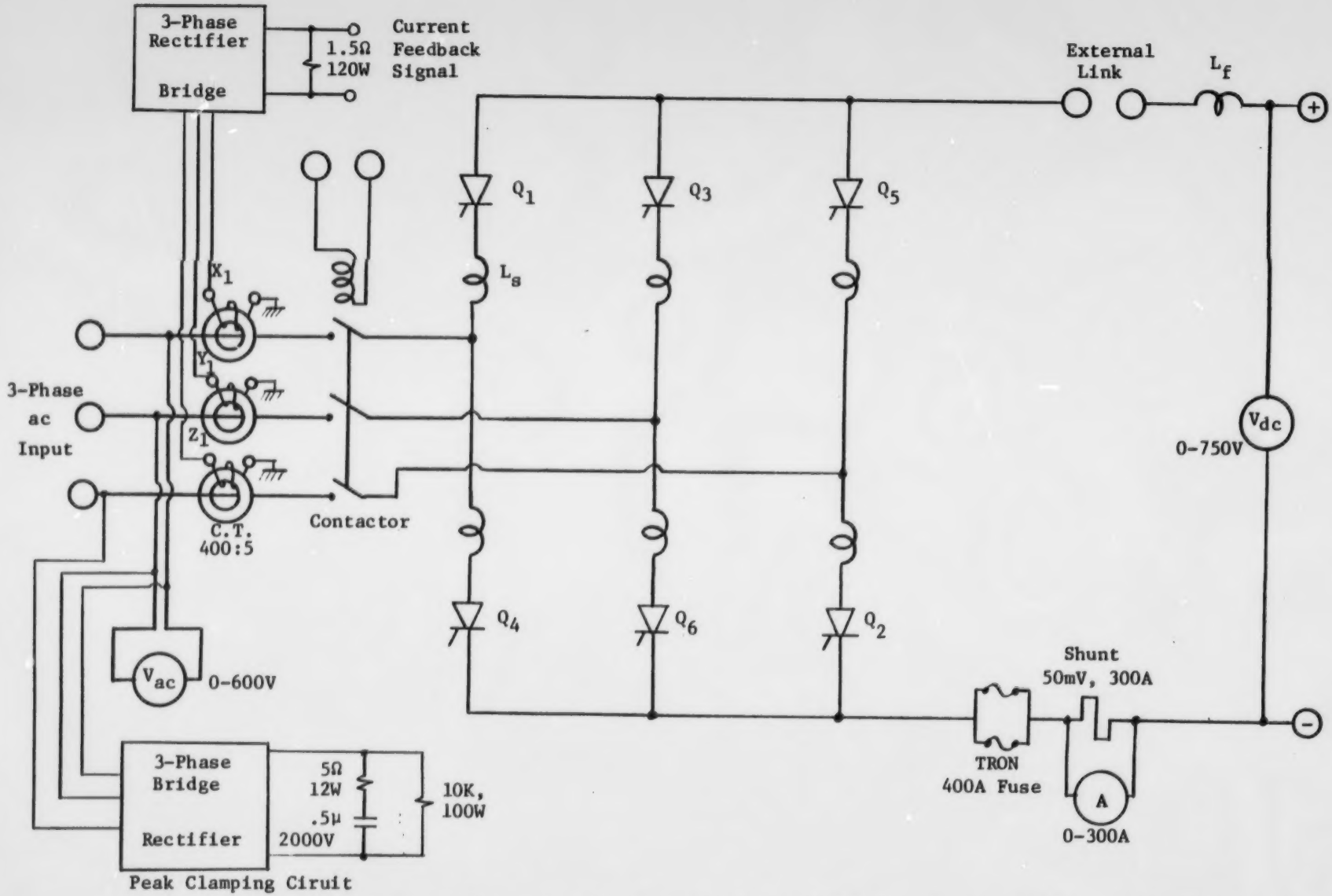


Figure A.8 Power circuit diagram of the "N" clamping controlled rectifier bridge.

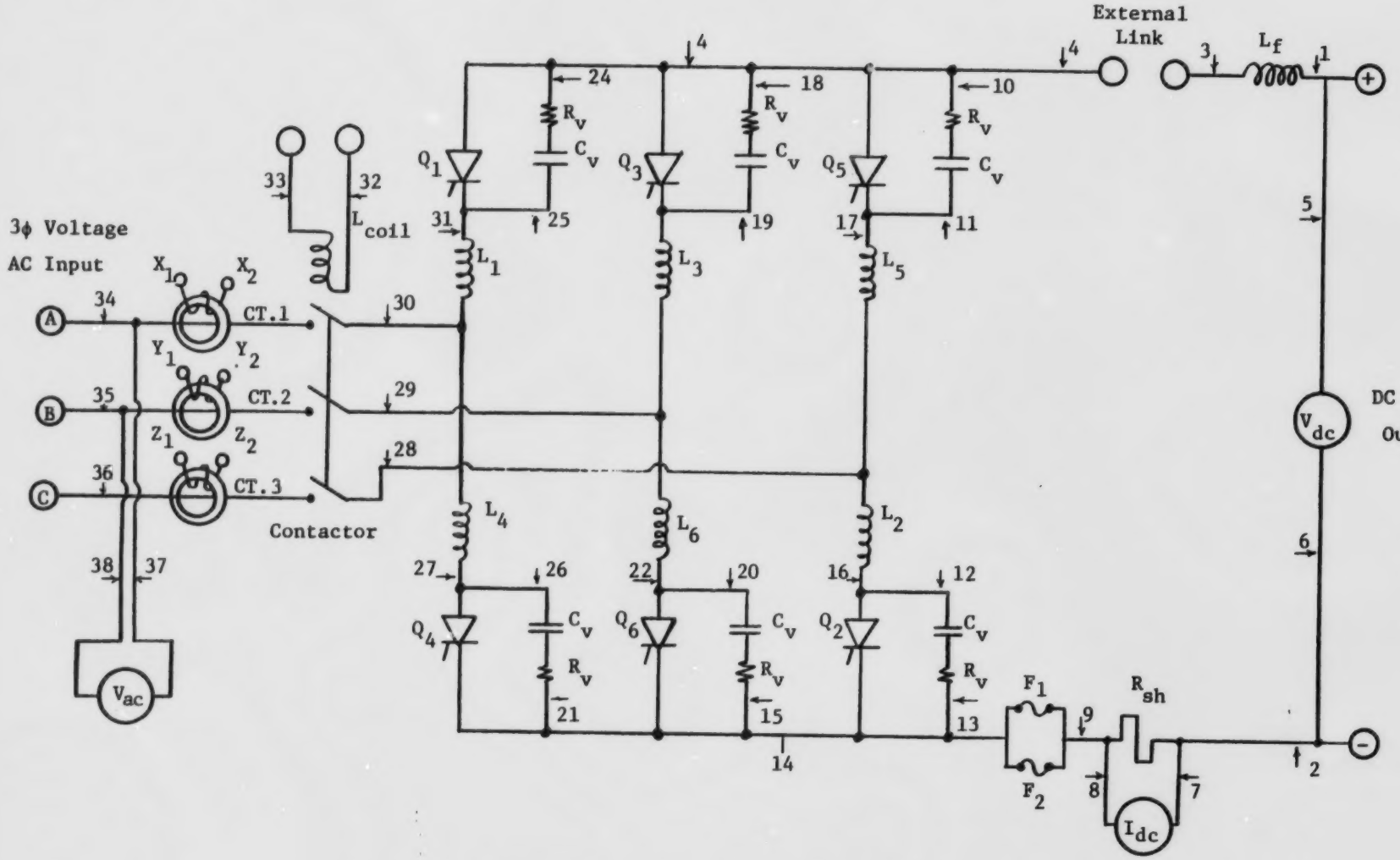


Figure A 9 NEGATIVE BRIDGE - DETAILED POWER CIRCUIT
The numbers indicate wires connecting different circuit components.

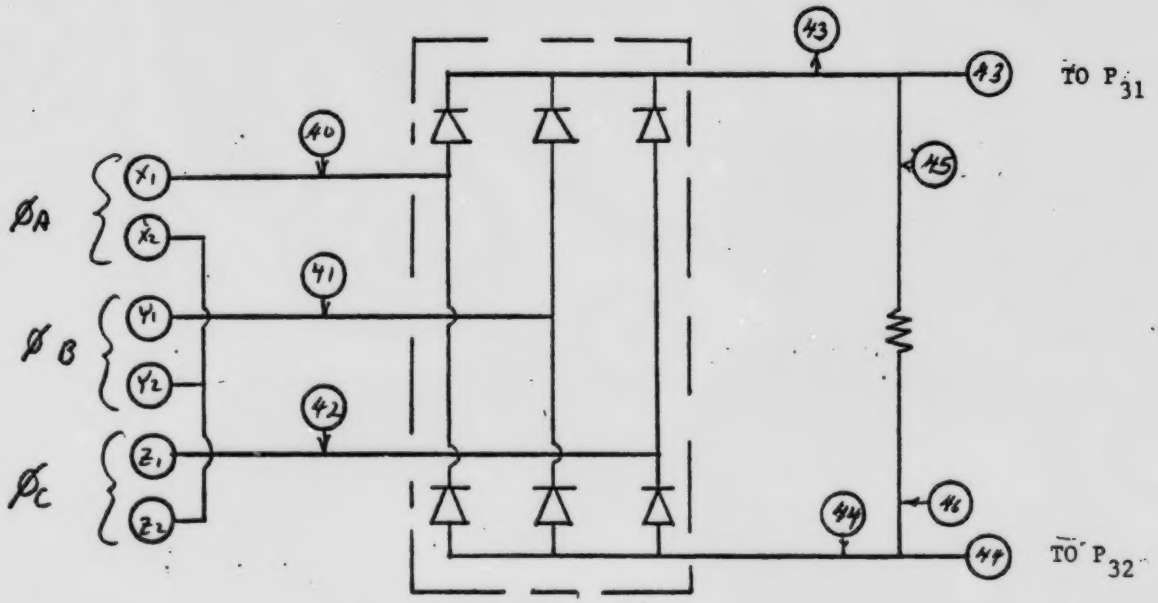


Figure A.10 CURRENT FEEDBACK - CLAMPING UNIT

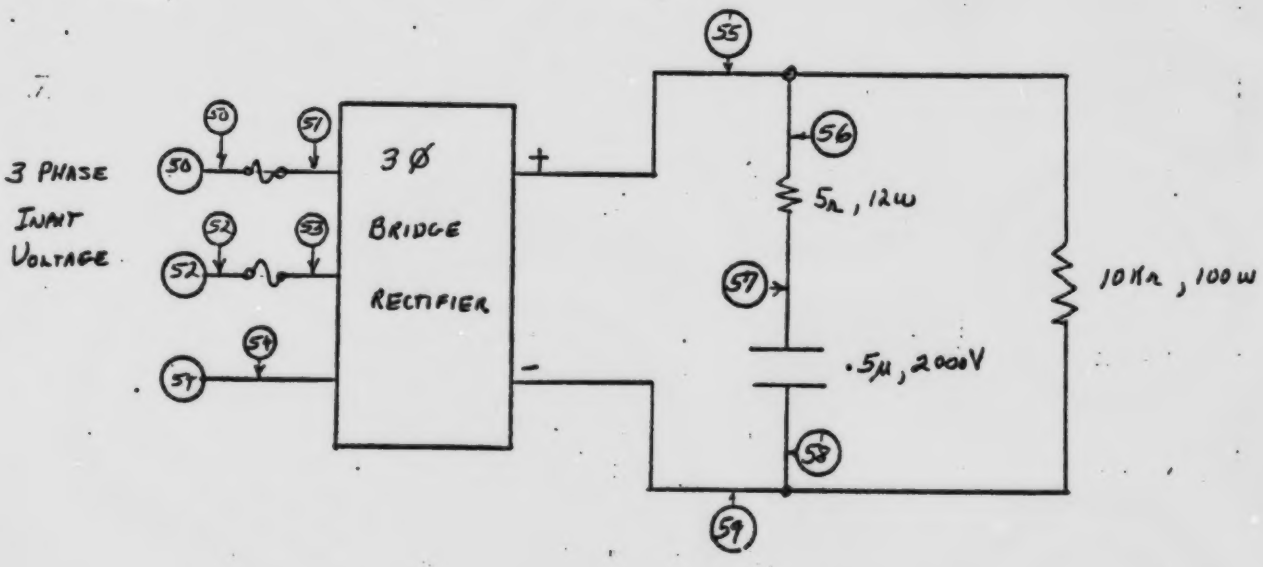


Figure A.11 PEAK VOLTAGE CLAMPING - CLAMPING UNIT

Table A3

Specifications of the components of "N" damping controlled rectifier bridge (Figure A 5)

S.N.	Component	
1	Thyristors (Q_1 to Q_6)	Westinghouse T720223504, 300 A, 1200 V
2	Current transformer (C.T.)	Westinghouse 145P667H01
3	Series inductor, L_1	7 μH, 350 A
4	Snubber networks, R_v C_v	10 Ω, 50 W non inductive ohmite 0.2 μF, 1000 V WIHA capacitors
5	Filter inductor, L_f	2.0 mH, 400 A 2 in series of 45 turns, 14" diameter
6	Magnetic contactor	135 A, 600 V

A 3.5 Logic and Control Circuits

Each controlled rectifier bridge (Figure A1) is controlled by a logic and control circuit, which provides gating signals to the bridge thyristors. Since the logic and control circuits for the "P" and the "N" bridges are identical, only one of them is described.

Figure A:12 shows the block diagram of the logic and control circuits. The circuits provides six 240° wide gating signals for each thyristor. The function of each block in Figure A12 is described below.

(1) 3-Phase Voltage Sensing: A delta-star 3-phase transformer is used to sense the input voltage of the rectifier bridge. This signal establishes the reference for phase angle delay, β and reduces the input ac voltage to the logic level.

(2) 60° Phase Shift: An R-C network is used to provide filtering of the voltage spikes on the input lines. The phase shift of 60° also provides a direct reference for phase angle β.

(3) Zero Crossing Detector: This circuit provides six, 180° wide signals, Q_1 to Q_6 in Figure A13. Signal Q_1 is at logical one when line voltage V'_{ab} is positive. Signals Q_1 to Q_6 are sequentially delayed from the previous signal by 60°.

(4) Sequential 60° Decoding: The signals Q_1 to Q_6 are processed by logic gates to obtain six signals which are 60° wide and phase displaced from each other by 60° (Figure A13).

(5) Digital β Processing: This unit provides an adjustable delay angle for gating the thyristors. The circuit consists of six similar circuits for producing gating signals for the six bridge thyristors. Figure A14 shows the block diagram for one of the six circuits of the processor. The circuit consists of a high frequency V.C.O. and

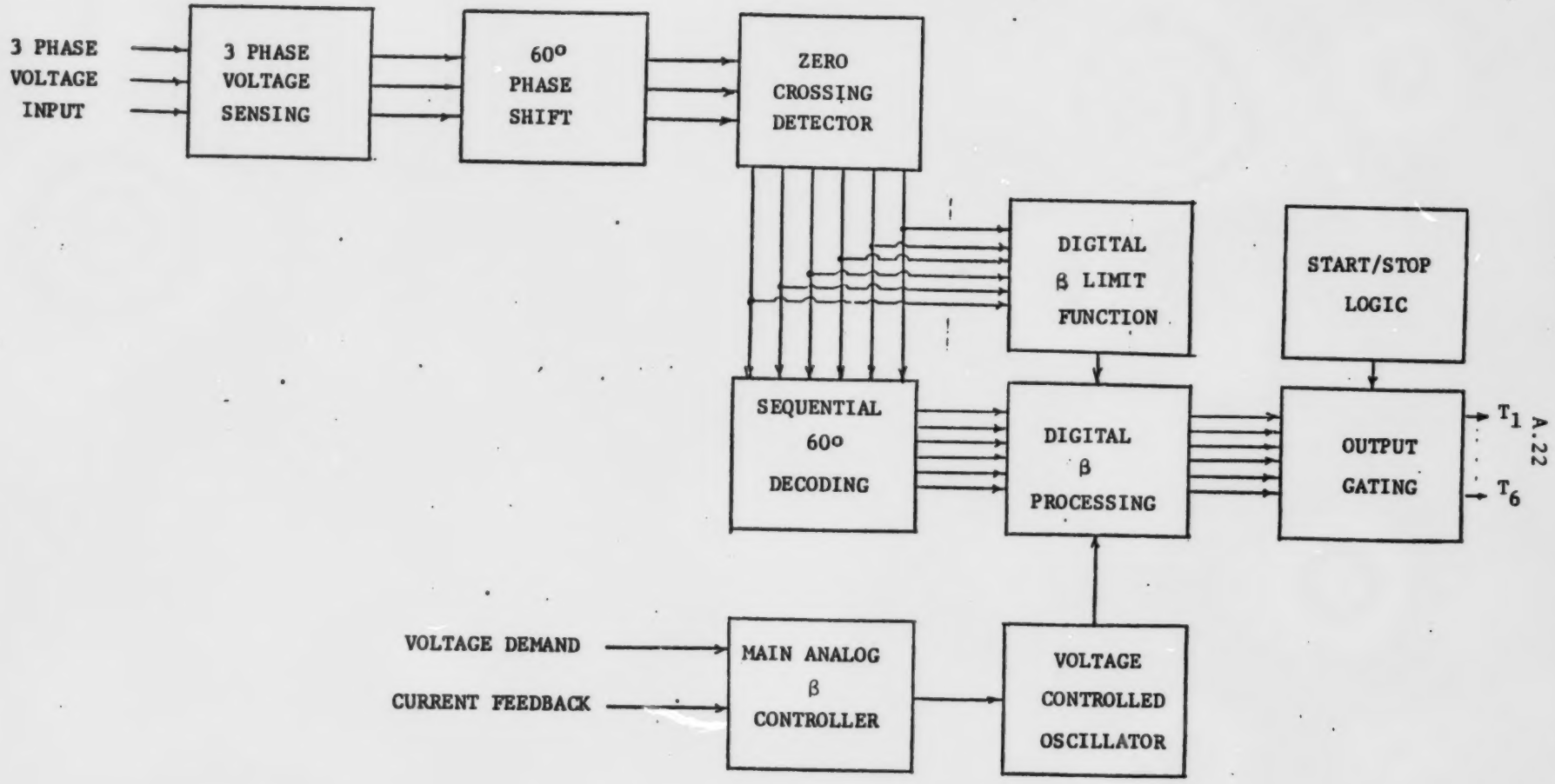


Figure A 12 PHASE CONTROL LOGIC - BLOCK DIAGRAM

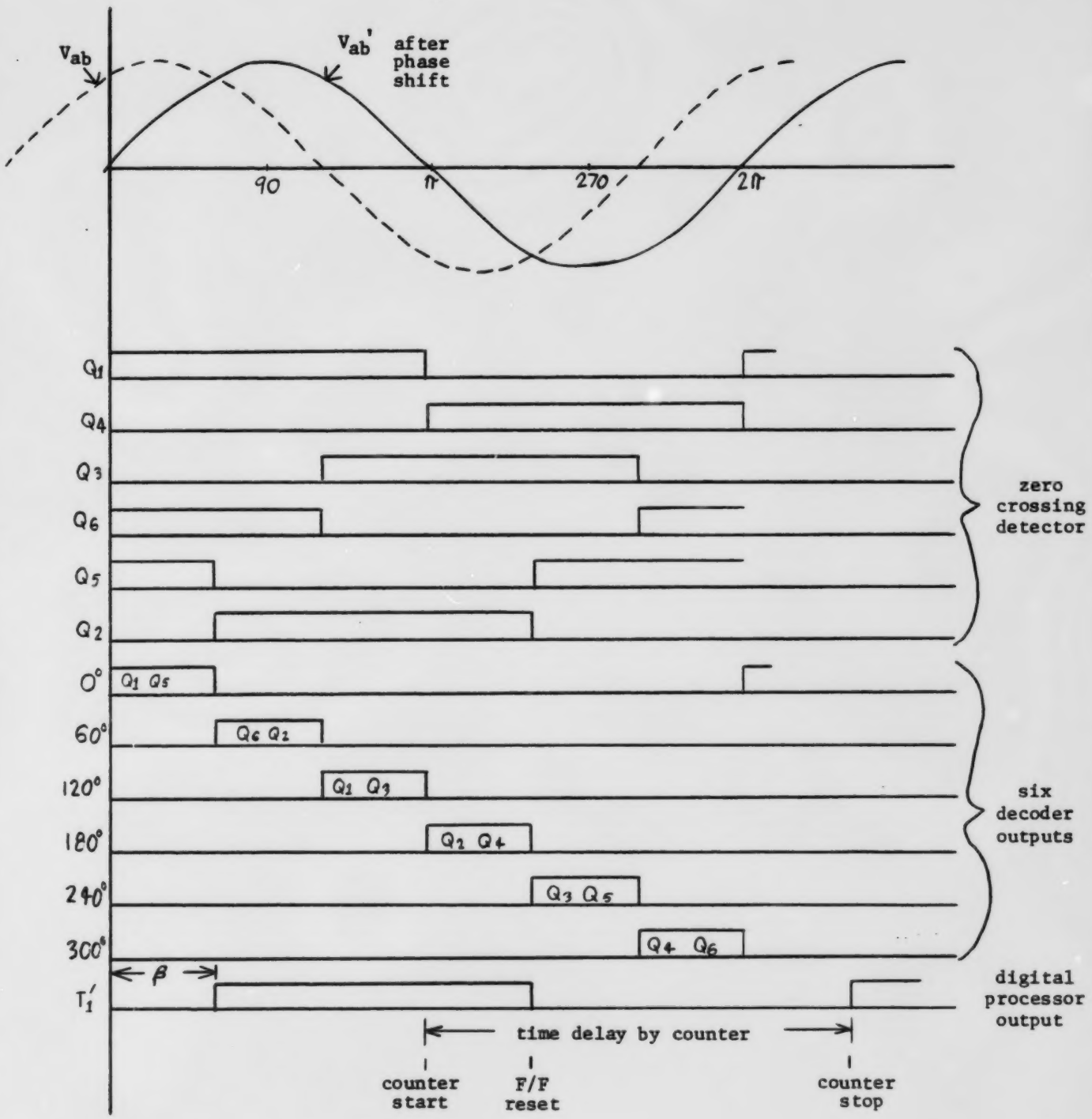


Figure A.13 Output waveforms for the block diagram of Figure A12

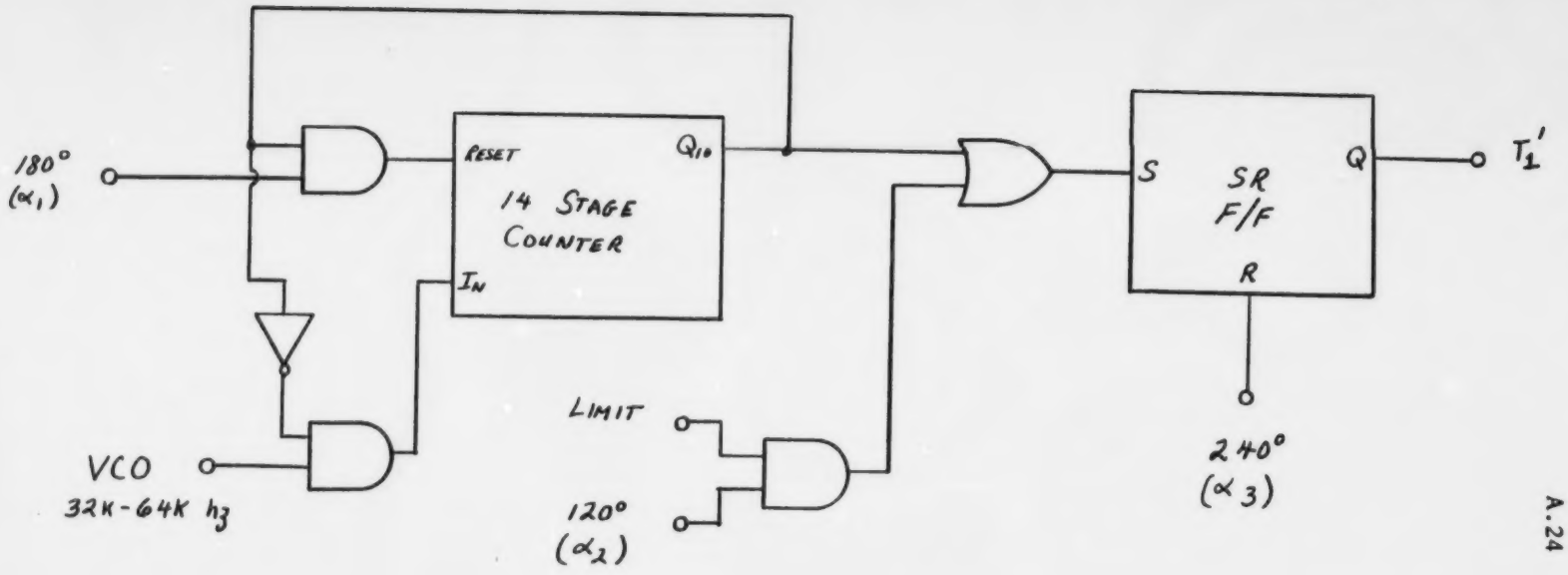


Figure A14 Block diagram showing one channel of the digital β processor.

a binary counter. The adjustable phase delay is provided by varying the frequency of the V.C.O. output. The counter is reset at 180^{o} (decoder output) and the counter starts counting. After a time interval ($>\pi$), depending upon the frequency of V.C.O., the output Q_{10} of the counter is set to logical one and it sets the output F/F. At the same time the input pulses to the counter are blocked. The output F/F is reset at 240^{o} (decoder output). The output signal T_1' thus starts at a variable angle, β, depending upon frequency of V.C.O. ($0 < \beta < \pi$) and is reset at 240^{o} (Figure A 13).

In order to provide sufficient turn off time for bridge thyristors, the delay angle is limited to a maximum value by a limit signal, which sets the F/F (Figure A 14) independent of the counter.

The remaining five channels of the digital processor are identical to Figure A 14 , except that angles α_1, α_2 and α_3 are advanced successfully by 60^{o}.

(6) Voltage controlled Oscillator (V.C.O.): This oscillator provides a variable frequency pulse train to the digital β processor. The frequency of the V.C.O. is determined by a dc control voltage. The control voltage can be derived from a potentiometer for manual control or an analog controller for closed loop feedback control.

(7) Digital β Limit Function: This circuit provides a pulse at adjustable angle (150^{o} - 170^{o}) to limit the value of the delay angle of the bridge. The limit function provides a common signal, at every 60^{o} interval for the six channels of the digital β processor. The appropriate limit interval is selected in the processor, such as 120 - 180^{o} (α_2) in Figure A14 . The β limit function produces digital pulses at 2^{o} intervals by a phase locked loop. The pulses are fed to a counter. The output of the counter is compared digitally to

an adjustable 4 bit digital word to generate the limit signal.

(8) Main Analog β Controller: The function of this circuit is to provide a dc control voltage to the voltage controlled oscillator (V.C.O.). The circuit consists of an inner proportional-integral (P-I) loop for regulating the dc output current of the rectifier bridge and an outer P-I loop for regulating the output voltage. The current feedback signal is provided by current transformers in the ac lines (Figure A7). The voltage feedback signal is obtained indirectly by producing a dc voltage proportional to the frequency of the V.C.O. This voltage is compared against a demand signal and the error is integrated by a P-I controller. The resulting signal is the reference to the inner current loop. The circuit also provides adjustable analog limits on the dc output which controls the V.C.O.

(9) Start/Stop Logic: This circuit provides a signal to inhibit or pass the gating signals through the output gating circuit. It also provides a signal to discharge the capacitor in the P-I controller for current regulation and to operate the indicator lights on the front panel.

(10) Output Gating: This circuit modulates the output signals of the digital β processor by the high frequency V.C.O. output and feeds them to the gate drive for the bridge thyristors. It also inhibits the gating signals when the 'stop' signal is present or an overcurrent condition is detected.

A 3.5.1 Layout of the Logic and Control Circuit

The hardware for the logic and control circuit of Figure A12 is constructed in different modules which are interconnected by coded wires to facilitate testing and debugging. Figure A15 shows the layout of different components which are briefly described below.

(1) Augut Boards A and B: The electronic integrated circuits (I.C.) of the logic are located on these boards. Each board is provided with a 36 pin edge connector to interconnect the signals to and from other circuits. Figure A16 and A17 show the layout of boards A and B respectively. The diagrams identify each IC by its type number (e.g. 4518) and its location by a letter (e.g. S). Thus, each I.C. can be rapidly located for testing. Tables A 4 and A5 give a list of the signals connected at the edge connectors of boards A and B respectively. The signals available on the edge connectors are referred as A1 to A36 and B1 to B36 respectively in the wiring diagrams. Table A6 lists direct interconnections between edge connectors A and B.

(2) Logic Strip, L: The wires from different modules are interconnected at the logic strip. These connections are referred as L_1 to L_{40} and are listed in Tables A7 and A8.

(3) Power Panel, P: The wires from the power circuits are interconnected to the logic circuits through the power panel. These connections are referred as P_1 to P_{40} and are listed in Table A9.

(4) Power Supply Module: This module provides at ± 15V and + 24 V to the logic circuits of boards A and B and the pulse amplifier module. The terminals of this module are referred as S_1 to S_8 (Figure A13).

(5) Pulse Amplifier Module: This module provides the driver stage to connect the output of the logic circuit (T_1 to T_6, in Figure A12)

to the gates of the thyristors.

(6) Front Panel, M: The indicating lights and potentiometer for voltage control are located on this panel. The connections to this are referred as M_1 to M_{12}.

(7) Relay Board: This module consists of triac circuitry for indicating lights. In the "N" controlled rectifier bridge also contains relay circuits for the opening and closing of the ac line contactor. The connections to this board are referred as RB-1 to RB-5. Since the circuit diagrams of the "P" and the "N" controlled rectifier are different, separate drawings are given for each circuit. In the "P" rectifier bridge, (detailed drawings 15 and 16) the start of the logic turns on the run light. The control voltage directly runs the power-on light and the cooling fan. In the "N" rectifier bridge (detailed drawings 17 and 18) in addition to the indicating lights and the fan, a rectifier bridge is used to provide power to the line contactor in the power circuit.

A 3.5.2 Detailed Drawings

The different blocks of the logic and control circuit, shown in Figure A 12 have been implemented according to the layout given in section A 3.5.1 Figure A18 shows the block diagram of Figure A12 , in detail. The interconnections of different blocks have been identified with numbers according to the layout plan of Figures A 18.

The circuitry for all blocks of Figure A18 have been documented on different drawings. A set of the drawings and their list is attached at the end of this section (Table A10).

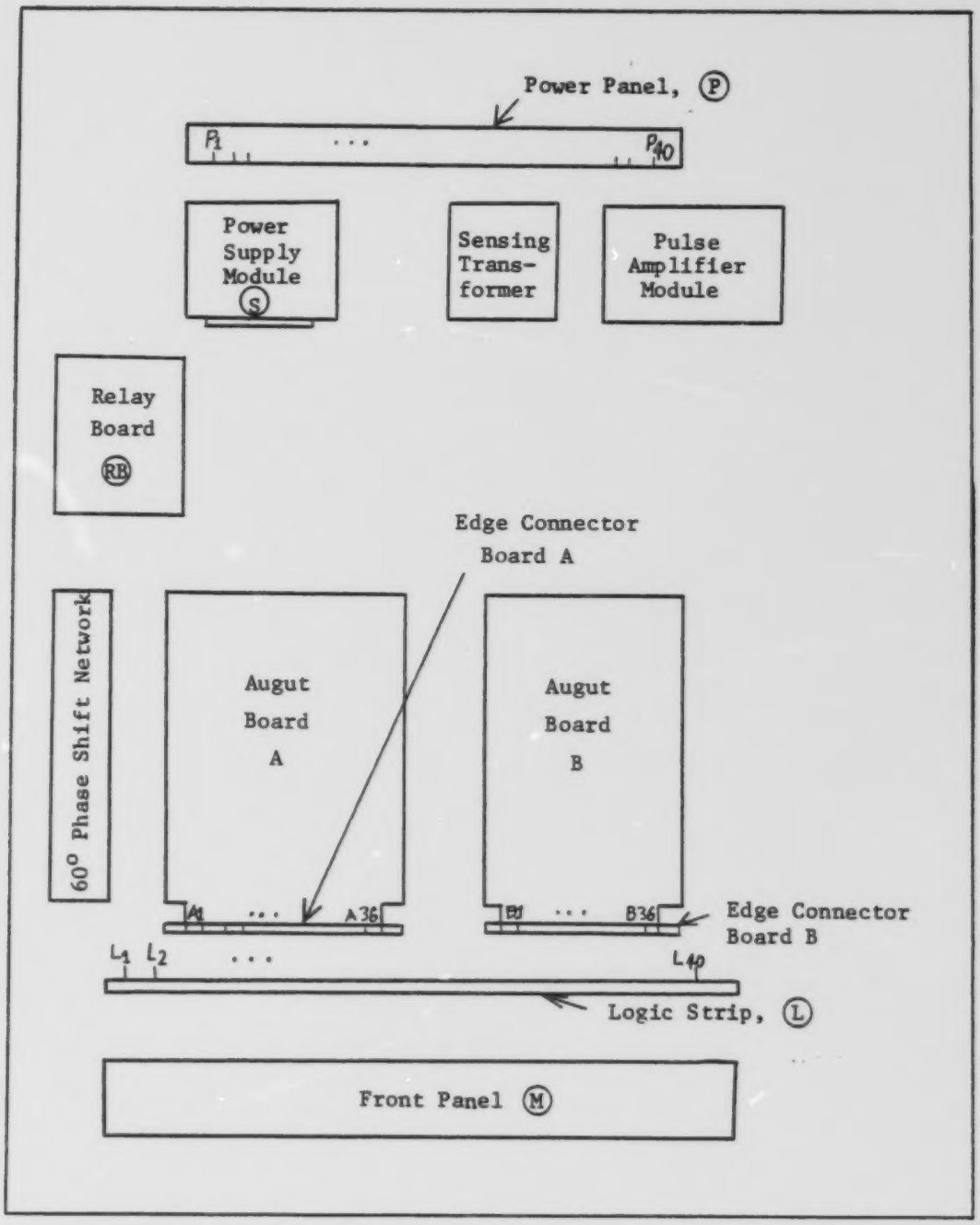


Figure A.15 The layout of the logic and control circuit. The circled letters, L, M, P, S and RB are used as prefixes in the wiring diagrams (D1 to D18) to indicate the connections. For example, L2 indicates connection on the logic strip at the second jack.

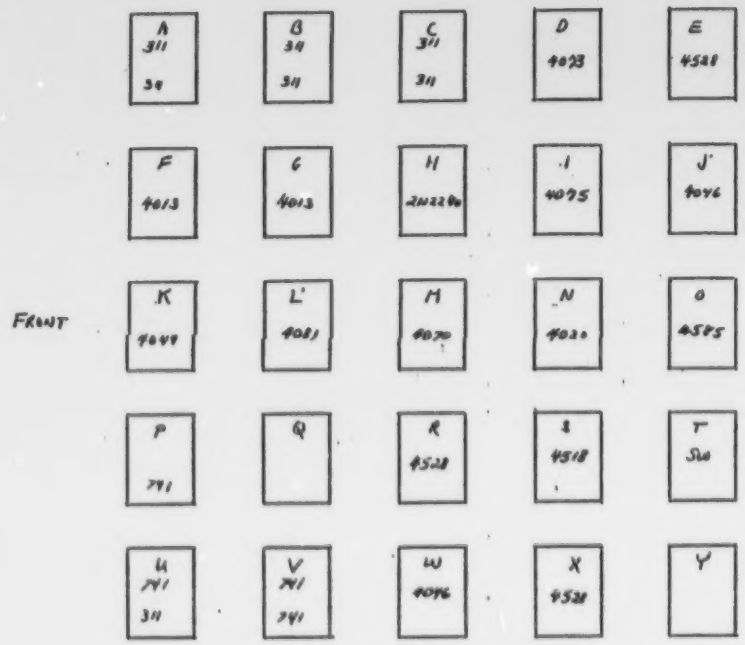


Figure A.16 ZERO CROSSING DETECTOR, DIGITAL β LIMIT, MAIN ANALOG β CONTROLLER, AND VOLTAGE CONTROLLED OSCILLATOR CIRCUIT LAYOUT - BOARD A

Table A.4

EDGE CONNECTOR BOARD A

1	ØA
2	ØB } 3Ø INPUT AFTER 60° SHIFT
3	ØC
4	N.A.
5	N.A.
6	To B-29 RUN-START = IAC=0
7	∠ MONITOR
8	LIMIT
9	My/L24 CT. OF CONTROL POT
10	CURRENT FEEDBACK P31/L20
11	L22 EXTERNAL CURRENT DEMAND
12	L28
13	L26
14	+15
15	GND
16	+15
17	GND
18	+15
19	GND
20	+15
21	GND
22	+15
23	GND
24	+15 VOLTS 'IN'
25	-15 VOLTS 'IN'
26	-15 V (INTERNAL)
27	$\overline{HF}$
28	Q_1
29	Q_2
30	Q_3
31	Q_4
32	Q_5
33	Q_6
34	OUTPUT SIGNAL 'OVER CURRENT' To B-28
35	To $\overline{MS}$/L25 OF EXTERNAL CONTROL POT
36	VCO

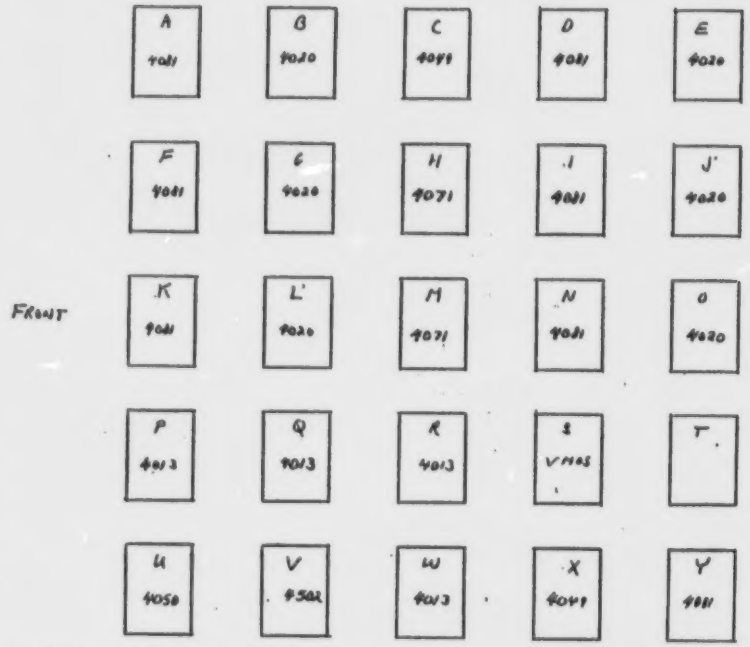


Figure A17 SEQUENTIAL 60° DECODING, DIGITAL β PROCESSING, OUTPUT GATING AND START/STOP CIRCUIT LAYOUT - BOARD B

Table A5

EDGE CONNECTOR BOARD B

1	Q_1
2	Q_2
3	Q_3
4	Q_4
5	Q_5
6	Q_6
7	
8	RUN LIGHT TRIAC #2
9	CONTACTOR TRIAC #1
10	
11	LIMIT and A8
12	VCO and A36
13	
14	+ RAIL
15	GND
16	+ RAIL
17	GND
18	+ RAIL
19	GND
20	+ RAIL
21	GND
22	+ RAIL
23	GND
24	+15 VOLT (T_{24})
25	
26	$\overline{HP}$ and A27
27	TO A-6 (INITIAL '0' VOLTS OUTPUT OF IP6)
28	FROM 311 OVERCURRENT A-34
29	START
30	STOP
31	T_1
32	T_2
33	T_3
34	T_4
35	T_5
36	T_6

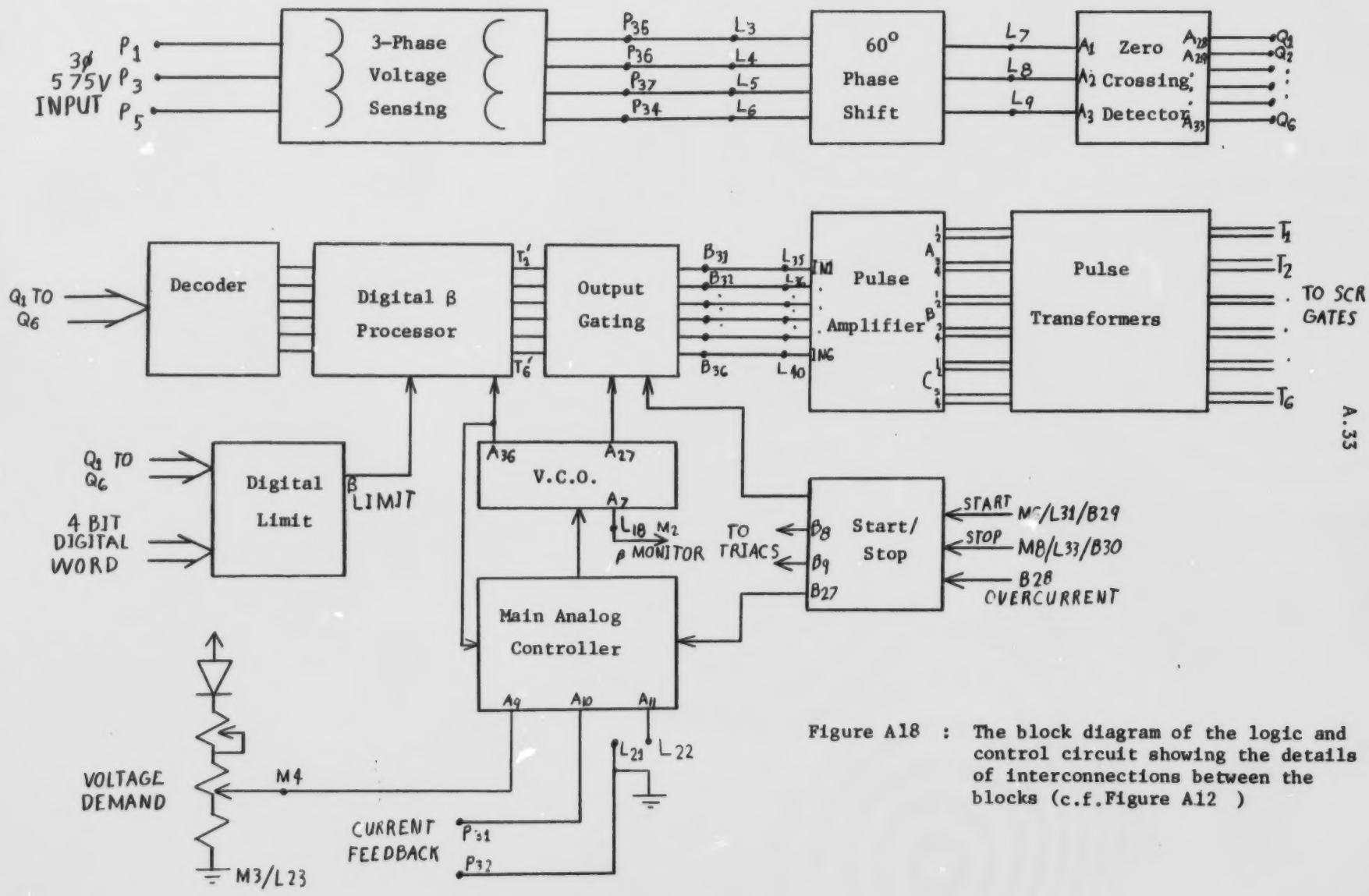


Figure A18 : The block diagram of the logic and control circuit showing the details of interconnections between the blocks (c.f.Figure A12)

Table A 6

AUGAT BOARD INTERCONNECTION

BOARD A	BOARD B
1	
2	
3	
4	
5	
6	27
7	
8	11
9	
10	
11	
12	
13	
14	
15	
16	
17	
18	
19	
20	
21	
22	
23	
24	
25	
26	
27	26
28	1
29	2
30	3
31	4
32	5
33	6
34	28
35	
36	12

Table A.7

LOGIC TERMINAL STRIP CONNECTION - RECTIFIER

DESTINATION	L-STRIP	LOGIC BOARD
S_1, RB-5	L_1	
S_2, M_{10}, M_{12}	L_2	
P_{35}	L_3	RC_{AI}
P_{36}	L_4	RC_{BI}
P_{37}	L_5	RC_{CI}
P_{34}	L_6	RC GND
	L_7	RC_{AO}
	L_8	RC_{BO}
	L_9	RC_{CO}
S_3, P_{21}	L_{10}	
S_4, RB-4	L_{11}	A_{24}, B_{24}
S_5, P_{22}	L_{12}	A-23, B-23
S_6, P_{23}	L_{13}	A-25
P_{28}	L_{14}	
P_{29}	L_{15}	
	L_{16}	
M_1	L_{17}	
M_2	L_{18}	A-7
	L_{19}	
P_{31}	L_{20}	A-10
P_{32}	L_{21}	
	L_{22}	A-11
M_3	L_{23}	
M_4	L_{24}	A-9
M_5	L_{25}	A-35
	L_{26}	A-13
	L_{27}	
	L_{28}	A-12
RB-3	L_{29}	B-8
	L_{30}	
M_6	L_{31}	B-29
M_7	L_{32}	
M_8	L_{33}	B-30
P_{26}	L_{34}	
IN-1	L_{35}	B-31
IN-6	L_{36}	B-32
IN-5	L_{37}	B-33
IN-4	L_{38}	B-34
IN-3	L_{39}	B-35
IN-2	L_{40}	B-36

Table A.8

LOGIC STRIP SPECIFICATION

L-STRIP	SPECIFICATION
L_1	110 VAC SUPPLY
L_2	110 VAC RETURN
L_3	3Ø INPUT ØA
L_4	3Ø INPUT ØB
L_5	3Ø INPUT ØC
L_6	GND of 3Ø INPUT AND 3Ø OUTPUT AFTER 60° SHIFT
L_7	3Ø OUTPUT ØA
L_8	3Ø OUTPUT ØB
L_9	3Ø OUTPUT ØC
L_{10}	+28V
L_{11}	+15V
L_{12}	GND
L_{13}	-15V
L_{14}	PHASE CONTROL OUTPUT VOLTAGE IN +
L_{15}	PHASE CONTROL OUTPUT VOLTAGE IN -
L_{16}	PHASE CONTROL OUTPUT VOLTAGE OUTPUT
L_{17}	∝ - MONITOR GND
L_{18}	∝ - MONITOR SIGNAL
L_{19}	
L_{20}	C.T. CURRENT SIGNAL +IN
L_{21}	C.T. CURRENT SIGNAL -IN & GND.
L_{22}	EXTERNAL COMMAND
L_{23}	CONTROL POT GND
L_{24}	CONTROL POT IN (WIPER)
L_{25}	CONTROL POT +15V
L_{26}	EC CONTROL IN/OUT (NORMAL SHORT L_{24} TO L_{28})
L_{27}	EC CONTROL EC +
L_{28}	EC CONTROL EC -
L_{29}	TRIAC #2 GATING (RUN LIGHT)
L_{30}	
L_{31}	START/STOP
L_{32}	START/STOP
L_{33}	
L_{34}	OVER VOLTAGE TRIP
L_{35}	T_1 OUTPUT GATING SIGNALS TO FIRE AMPLIFIERS.
L_{36}	T_2 OUTPUT GATING SIGNALS TO FIRE AMPLIFIERS.
L_{37}	T_3 OUTPUT GATING SIGNALS TO FIRE AMPLIFIERS.
L_{38}	T_4 OUTPUT GATING SIGNALS TO FIRE AMPLIFIERS.
L_{39}	T_5 OUTPUT GATING SIGNALS TO FIRE AMPLIFIERS.
L_{40}	T_6 OUTPUT GATING SIGNALS TO FIRE AMPLIFIERS.

Table A.9

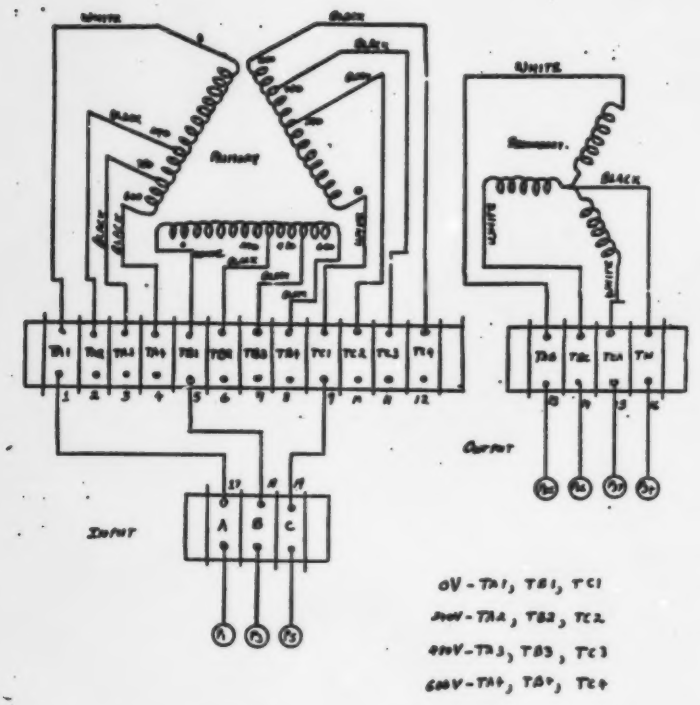
CONTROL PANEL SPECIFICATION

P_{21}	To L_{10} (+28V)	P_1	ØA To (1) Of Power Circuit
P_{22}	To L_{12} (GND)	P_2	ØB To (2) Of Power Circuit
P_{23}	To L_{13} (-15v)	P_3	ØC To (3) Of Power Circuit
P_{24}		P_4	
P_{25}		P_5	
P_{26}	To L_{34}	P_6	
P_{27}		P_7	
P_{28}	To L_{14}	P_8	
P_{29}	To L_{15}	P_9	
P_{30}		P_{10}	
P_{31}	To L_{20} (+) } From C.T.	P_{11}	
P_{32}	To L_{21} (-) } From C.T.	P_{12}	
P_{33}		P_{13}	
P_{34}	To L_C (GND)	P_{14}	
P_{35}	To L_3 ØA	P_{15}	
P_{36}	To L_4 ØB	P_{16}	
P_{37}	To L_5 ØC	P_{17}	
P_{38}	To RB-1 (Fan Supply)	P_{18}	
P_{39}		P_{19}	
P_{40}	To L_2 (Fan Return)	P_{20}	

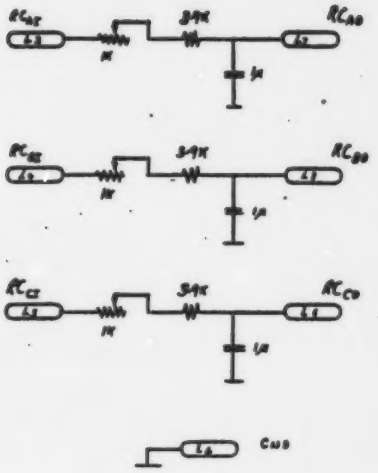
Table A 10

List of Detailed Drawings

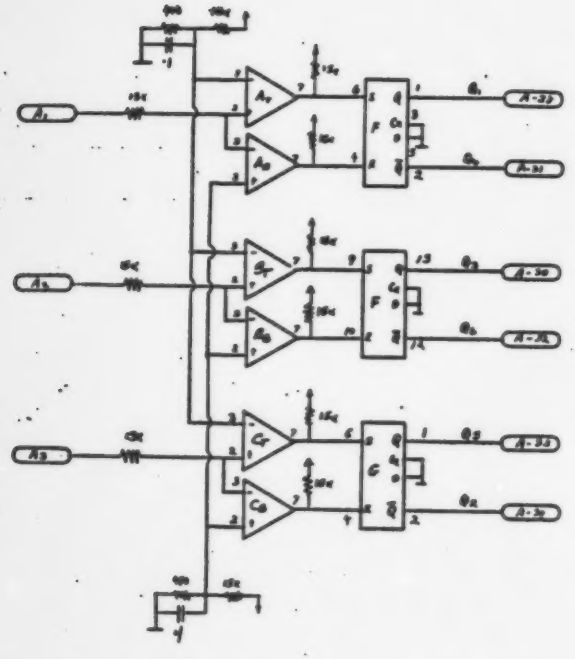
D1	3-Phase Voltage Sensing Transformer
D2	60^{o} Phase Shift Network
D3	Zero Crossing Detector
D4	Sequential 60^{o} Decoder
D5	Digital β Processing
D6	Output Gating
D7	Start/Stop Logic
D8	Voltage Controlled Oscillator
D9	Main Analog β Controller
D10	Digital β Limit Function
D11	Pulse Amplifier Circuit
D12	Pulse Amplifier Wiring
D13	Power Supply Wiring
D14	Front View of Front Panel
D15	Front Panel Wiring (P Bridge)
D16	Power on Light, Run Light and Fan Circuitry (P Bridge)
D17	Front Panel Wiring (N Bridge)
D18	Power on Light, Run Light and Fan Circuitry (N Bridge)



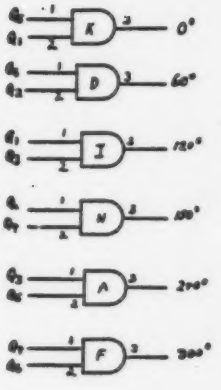
D1 3-Phase Voltage Sensing Transformer



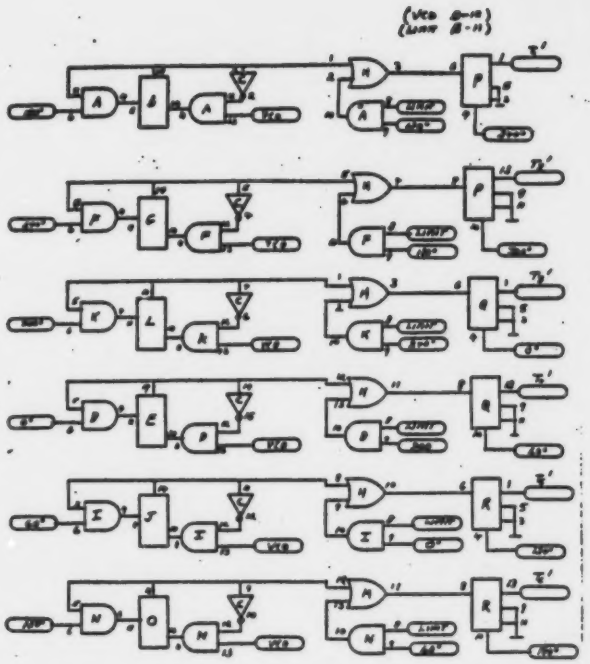
D2 60° Phase Shift Network



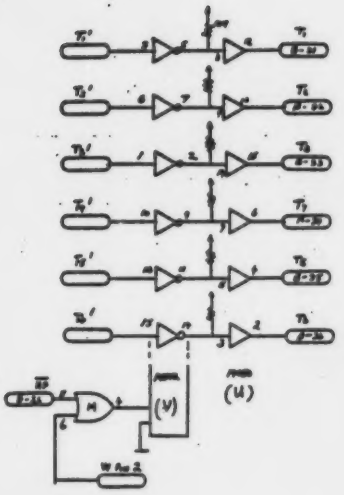
D3 Zero Crossing Detector



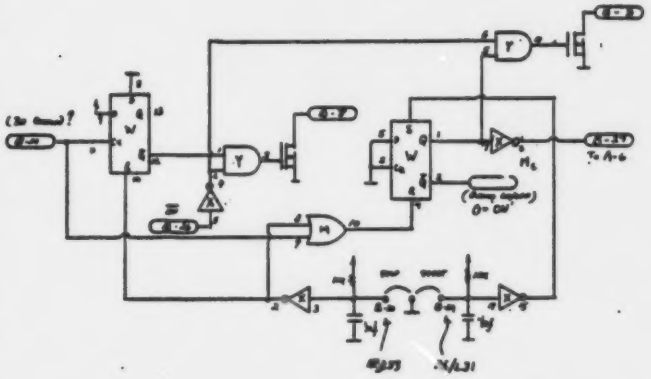
D4 Sequential 60° Decodor



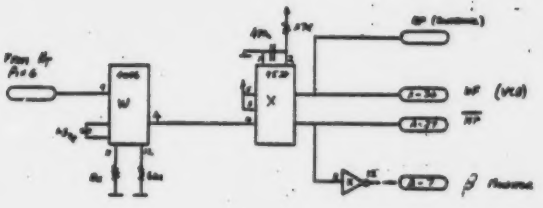
D5 Digital β Processing



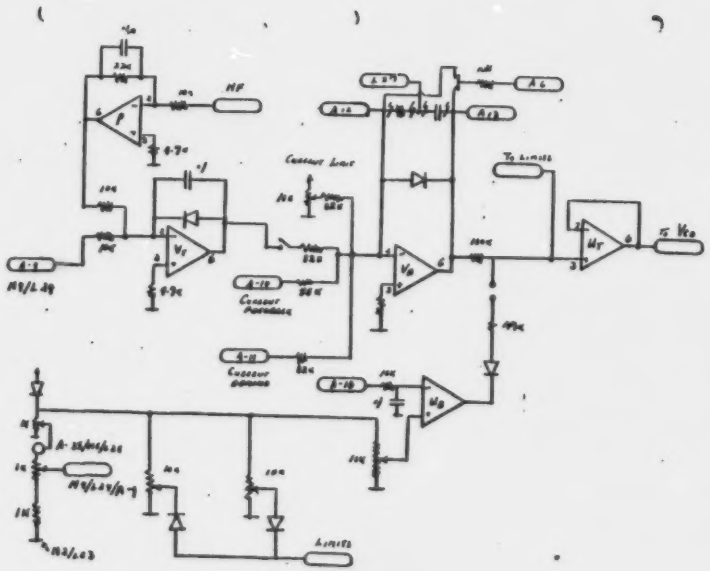
D6 Output Gating



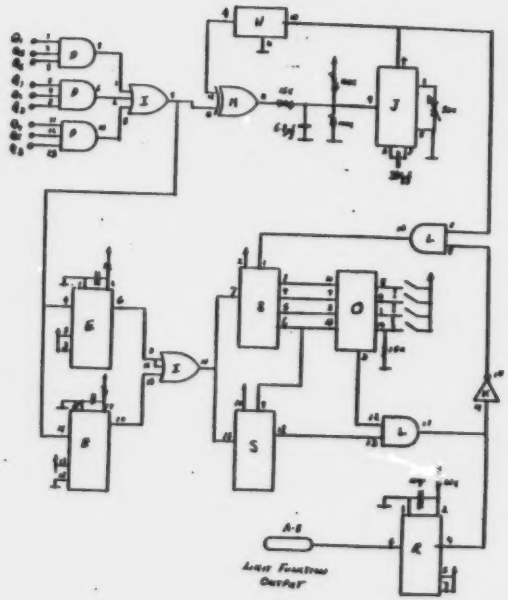
D7 Start/Stop Logic



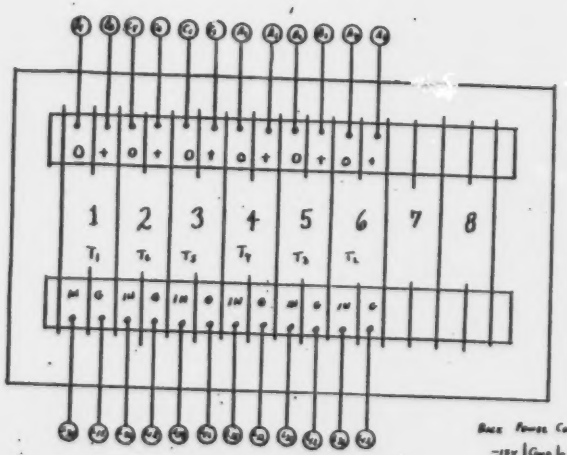
D8 Voltage Controlled Oscillator



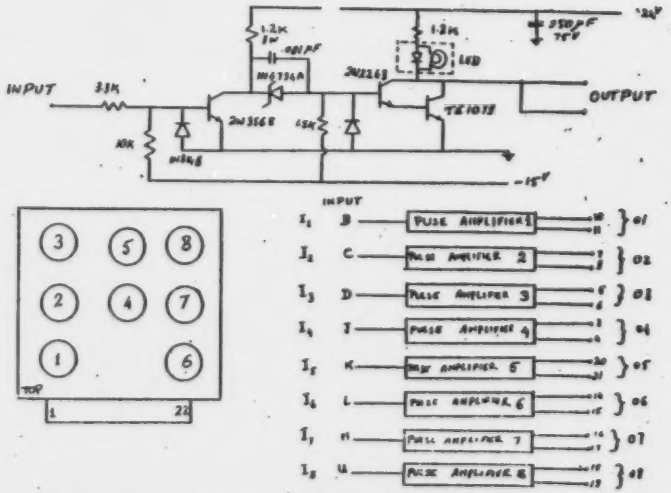
D9 Main Analog β Controller



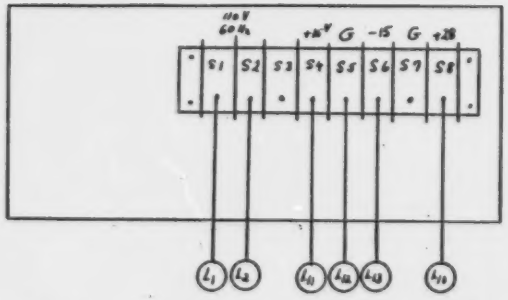
D10 Digital β Limit Function



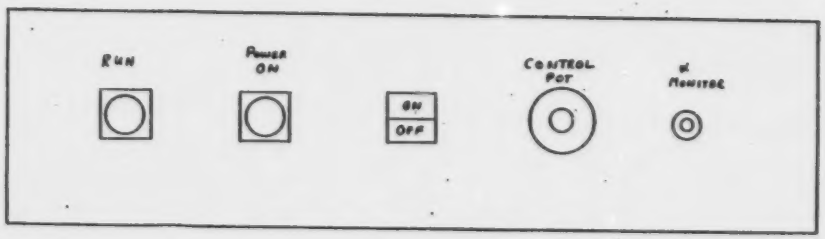
D11 Pulse Amplifier Wiring Rectifier Unit



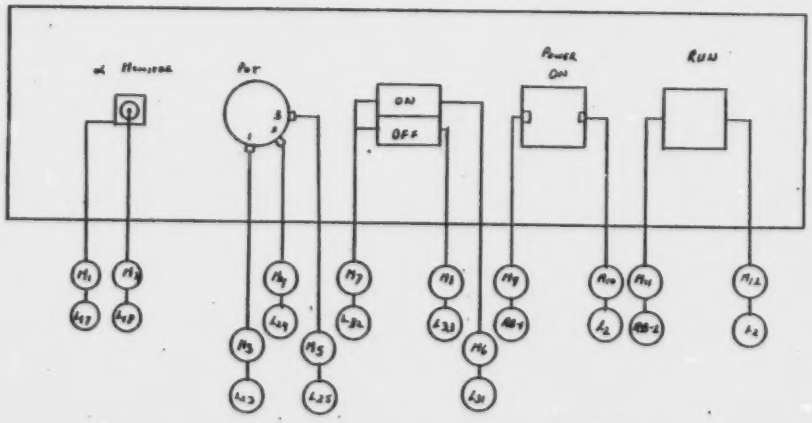
D12 Pulse Amplifier



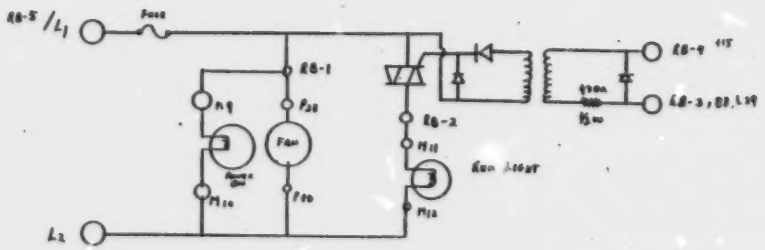
D13 Power Supply Wiring - Rectifier Unit



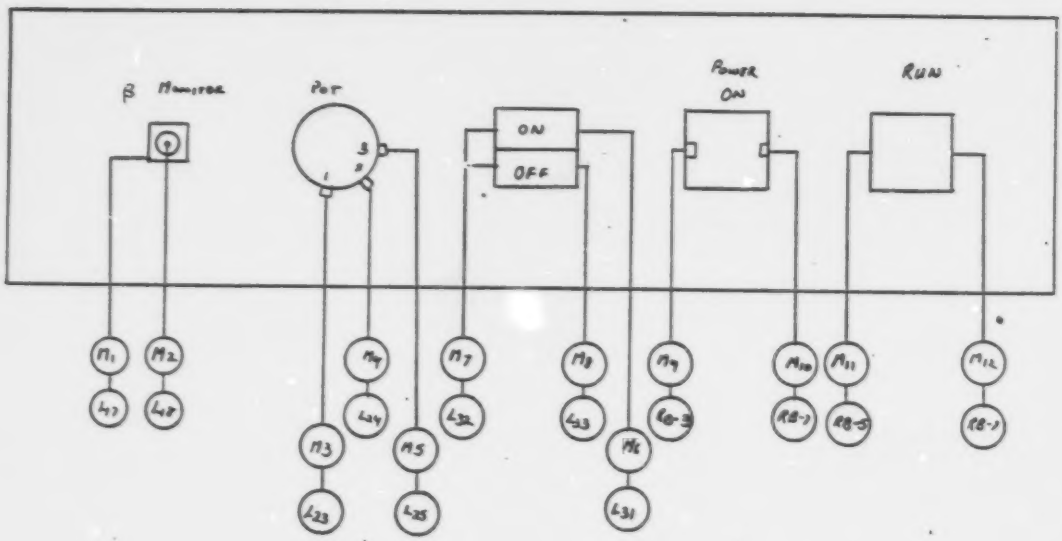
D14 Front View of Front Panel - Rectifier Unit



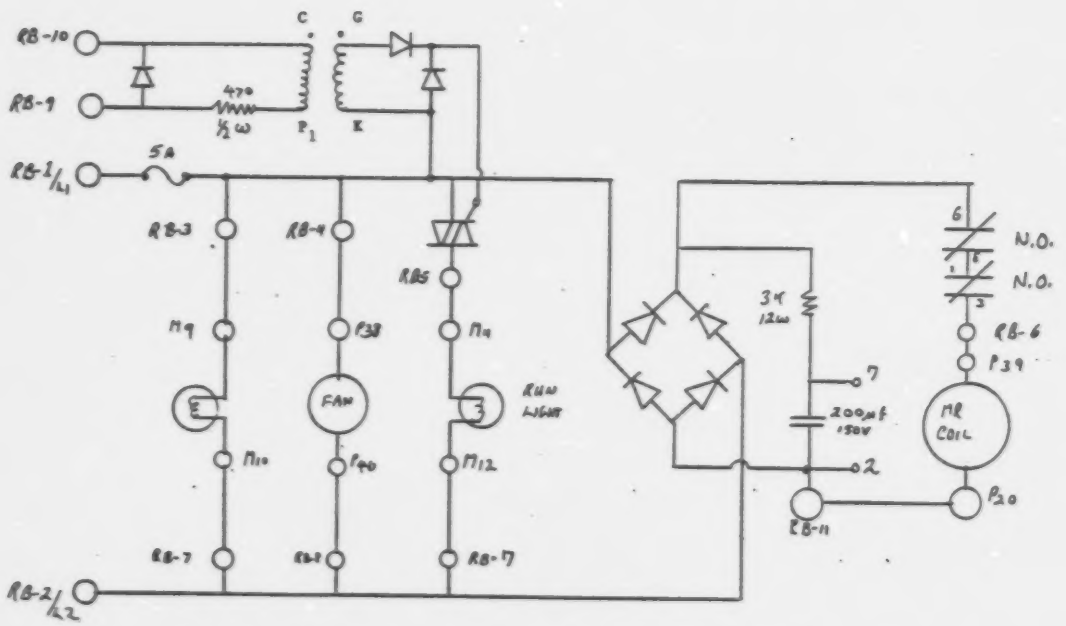
D15 Rectifier Unit - Front Panel Wiring



D16 Rectifier Unit: Power on Light, Run Light, and Fan - Circuitry.



D17 Clamping Unit - Front Panel Wiring



D18 Clamping Unit: Power on Light, Run Light, Fan, and Contactor - Circuitry.

APPENDIX B

LOADING UNIT

APPENDIX B

LOADING UNIT

B1 Introduction

The overall test set-up requires (Fig. 1.1) two loading units each capable of providing up to 125 Kilowatts to the separately excited dc machine (at 600 volts dc nominal) coupled to the 125 HP ac motor. A chopper unit for field control is also needed to obtain constant power loading in the constant power region of the speed-torque curve (Fig. 1.1). The loading unit must be capable of loading the ac motor in both motoring and braking regions.

B2 Specifications

The block diagram of one the loading units is shown in Figure B1. It consists of the following:

(a) A three-phase controlled rectifier to supply the armature of the loading machine,

(b) Filter inductor,

(c) DC chopper to supply the field.

The input to the unit is three-phase, 460 volt and the outputs are dc voltages for armature and field (both are independently controllable). The continuous rating of the armature supply is 125 kW at 600 volts dc nominal and the field unit can supply up to 10 kW up to 600 volts dc. The loading unit designed incorporates the following features:

(a) Protection against drop of input ac, overcurrent in armature, loss of field current, etc.

(b) Manual control and display of the output and input voltages and currents,

(c) All the relevant signals are brought down to logic levels in an isolated manner such that an interface with a data acquisition system can be made,

(d) The capability is provided such that the basic logic can be replaced with a microprocessor system,

(e) The capability of automatic control of the armature current and the armature voltage or speed (with inner current loop) has been provided,

(f) The capability of automatic control of the field current as a controlled function of the armature voltage can be implemented,

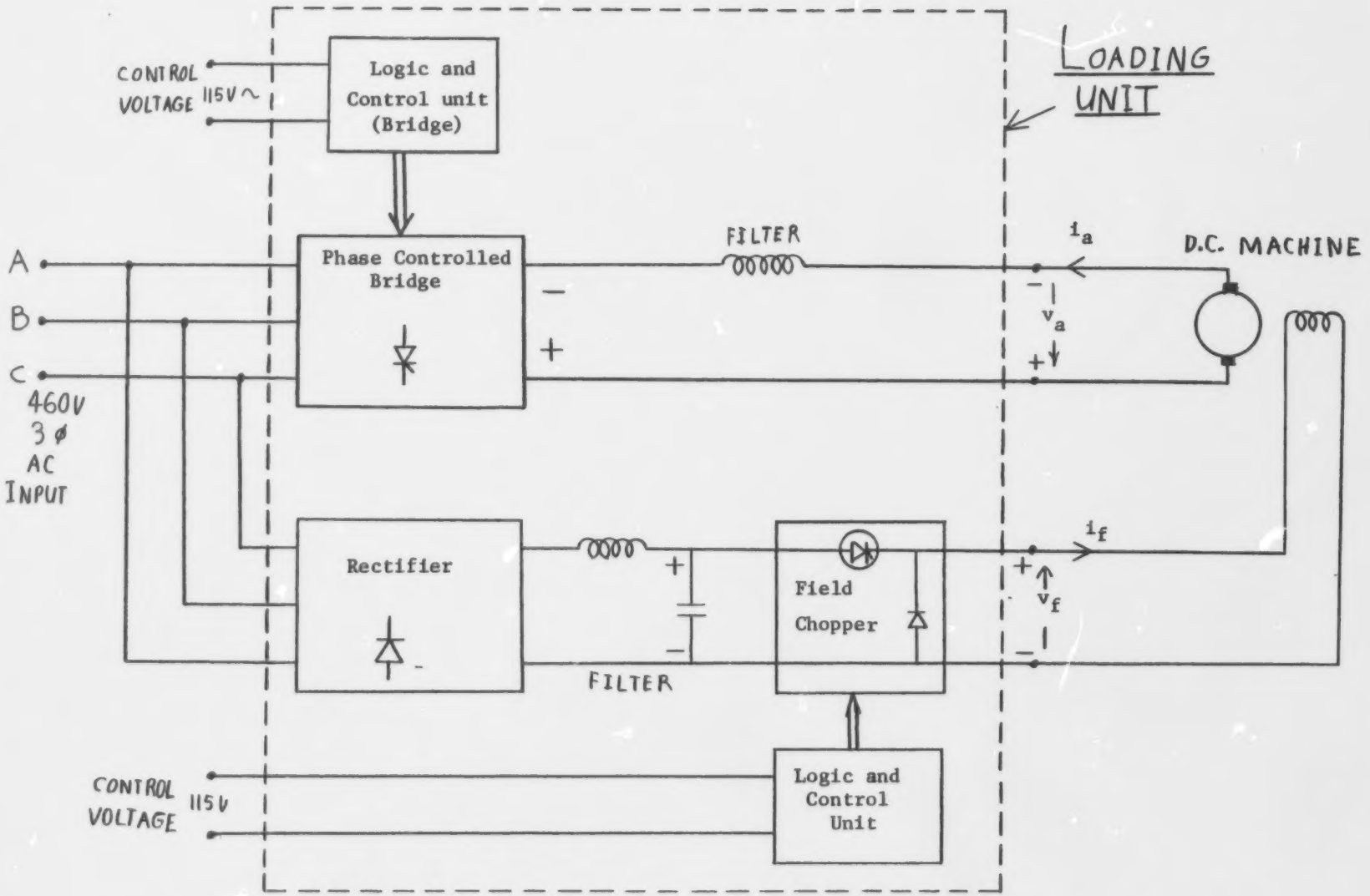


Figure B1 Block Diagram of the Loading Unit for the dc machine. The dc machine is used as a load on the ac squirrel cage motor mechanically coupled to it.

(g) The unit can provide static four quadrant loading with field reversal. Under dynamic conditions (field direction change is manual) only a two quadrant loading can be achieved.

In the next section the loading unit is explained in detail.

B3 DETAILED SYSTEM DESCRIPTION

The loading unit described in this section, converts power between the dc motor and the 460V secondary winding of the input transformer. The armature of the dc motor is connected to a phase controlled bridge and the field circuit is separately excited by a rectifier-chopper unit.

The block diagram of the loading unit was shown in Figure B1. The phase controlled bridge supplying the armature is capable of operating with positive or negative voltage and a unidirectional current. When the dc machine operates as a generator, it absorbs mechanical power from the inverter - ac motor system. The phase controlled bridge (Figure B1) then operates as an inverter and returns the power to the ac line. The phase controlled bridge can also be operated as a rectifier supplying power to the dc machine, when the ac machine is operating in the regenerating mode.

The field winding of the dc motor is excited from the 460 V ac supply through a rectifier-chopper unit. The uncontrolled rectifier converts ac supply to dc at a fixed voltage. The field current is controlled by a single quadrant, current commutated chopper.

The phase controlled bridge and the rectifier-chopper unit (Figure B1) are described in detail in the following.

B3.1 Phase Controlled Bridge

This unit is similar to the "N" controlled rectifier described in Appendix A , section A3. The detailed power circuit diagram of the phase controlled bridge for the loading unit is shown in Figure B2. A peak clamping circuit shown in Figure B3 is connected at the ac input lines. Figure B4 shows the current feedback circuit which rectifies the signal from the secondary of the current transformers. The rectified signal is connected to the logic and control unit.

Table B1 shows the specifications of the components used in the phase controlled bridge.

The logic and control unit for the loading unit controlled bridge is identical to that described for type "N" controlled bridge in Appendix A, section A3 . Therefore, Figures A16, A17 , detailed drawings D1 to D14, D17 and D18 and tables A4 to A8 given in Appendix A are also applicable to the phase controlled bridge of the loading unit.

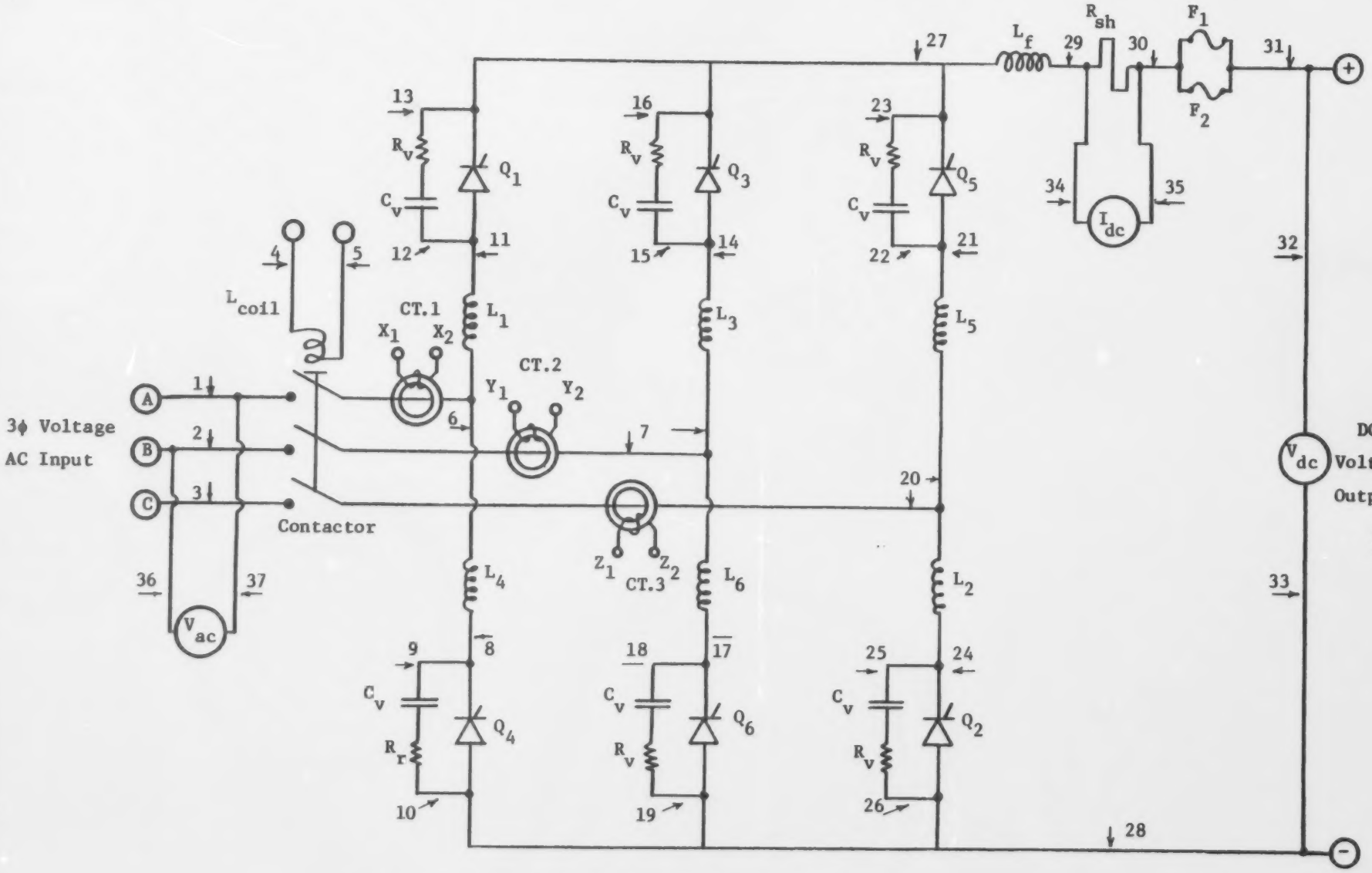


Figure B 2 LOADING UNIT - DETAILED POWER CIRCUIT

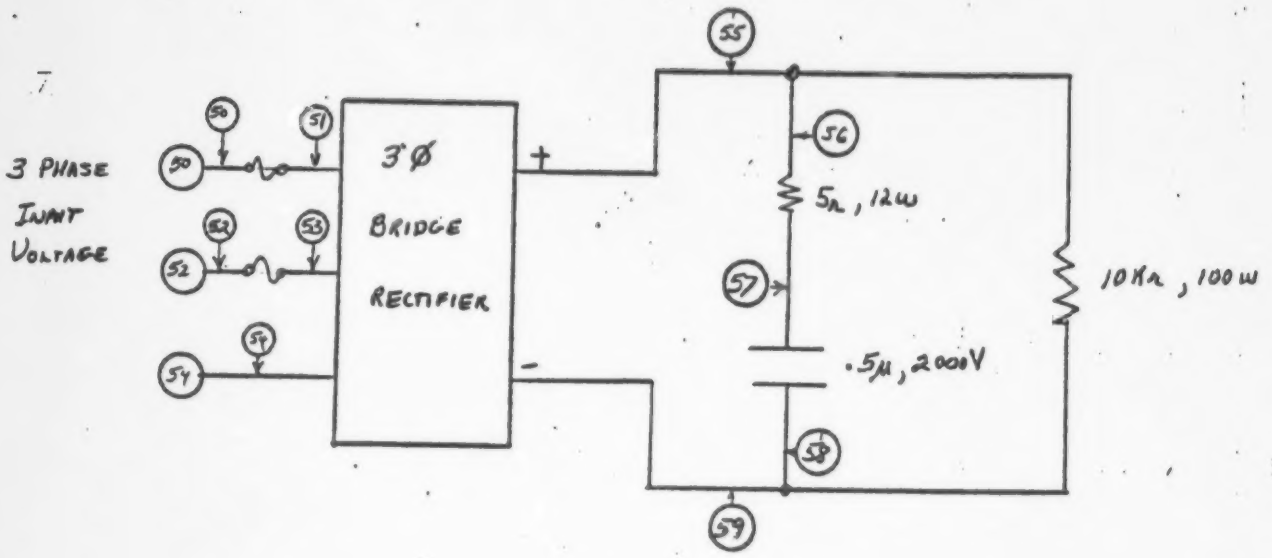


Figure B 3 PEAK VOLTAGE CLAMPING - LOADING UNIT

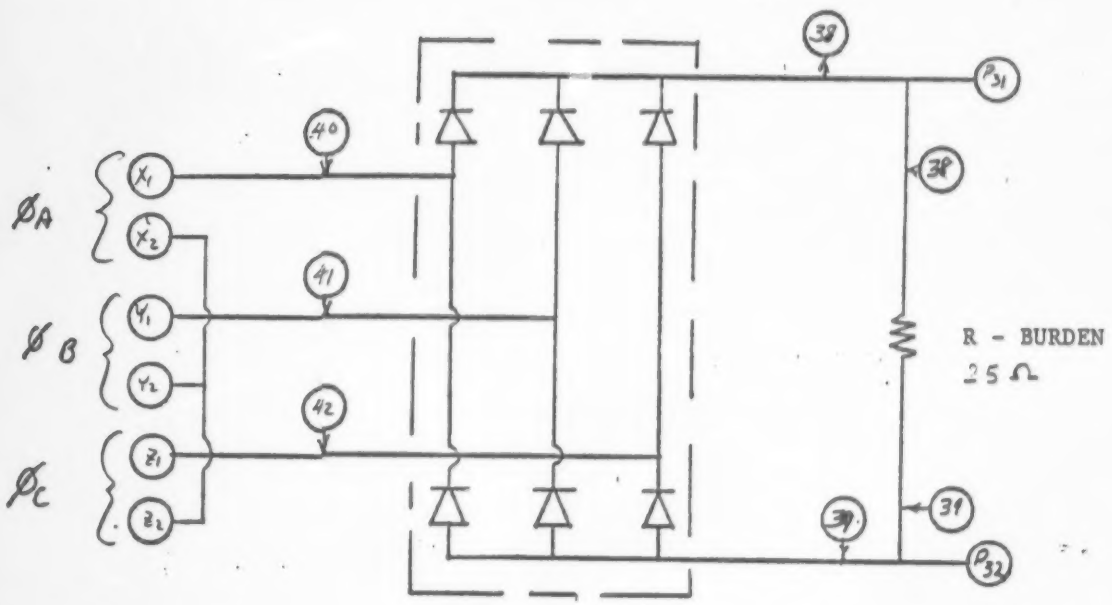


Figure B 4 CURRENT FEEDBACK - LOADING UNIT

Component	Specifications
Thyristors Q_1 - Q_6	Westinghouse, T620123004, 300A, 1200V, 100μs turn-off time
Series inductors L_1 - L_6	7μH, 350A, 10 turns
Current transformers	Westinghouse, 145P667H01, 400/ 5A
Snubber resistors R_v	10Ω, 50W, Ohmite
Snubber capacitors C_v	0.2μF, 1000V
Magnetic Contactor	Klockner Moeller, DIL-4-22-NA, 150A, 600V, 3ph., 60Hz
DC line fuse	Tron, 600V, 200A
Filter reactor, L_f	4 reactors in series, each 45 turns, ≈ 0.5mH
Voltmeter, AC	0 - 600V
Voltmeter, DC	750 - 0 - 750V
Ammeter, DC	0 - 300A, 50mV shunt

Table B1 Component specifications of the loading unit phase controlled bridge (Figure B2)

B3.2 Field Rectifier-Chopper

The loading unit includes a rectifier-chopper module which draws power from the 460V, 60Hz ac lines and supplies controlled current to the field winding of the dc machine.

Power Circuit Configuration: Figure B5 shows the power circuit configuration of the field rectifier-chopper. The input ac power at 460V, 60Hz is rectified by an uncontrolled rectifier bridge, D_1 to D_6 and filtered by L_f-C_f (Figure B5). A charging resistor R_{ch}, is included in series with L_f when the 3-phase ac power is turned on, to limit the charging current of the filter capacitor, C_f. After a time delay of four seconds resistor R_{ch} is shorted by a contactor. A freewheeling diode D_{rf} is connected in parallel with the inductor L_f to dissipate the stored energy. The filter capacitors C_f are also provided with discharge resistors R_f to dissipate stored energy when the power is turned off.

The single quadrant, current commutated chopper in Figure B5 consists of main thyristor Q_m, freewheeling diode D_f and the commutation circuit. The commutation circuit consists of inductor L_c, capacitor C_c, diode D_c, resistor R_c, and thyristor Q_c. The commutation is started by gating thyristor Q_c. Line inductor L_{IN} is used to limit di/dt when the main thyristor Q_m is turned on. Table B2 gives the specifications of the components of Figure B 5.

A Hall Effect current transducer is connected in series with the chopper output to provide the feedback signal for current regulation. A dc ammeter is also connected to indicate the average value of the output current.

The thyristor Q_m and Q_c in Figure B5 are gated by a logic and control circuit to control the output voltage of the chopper by pulse width modulation.

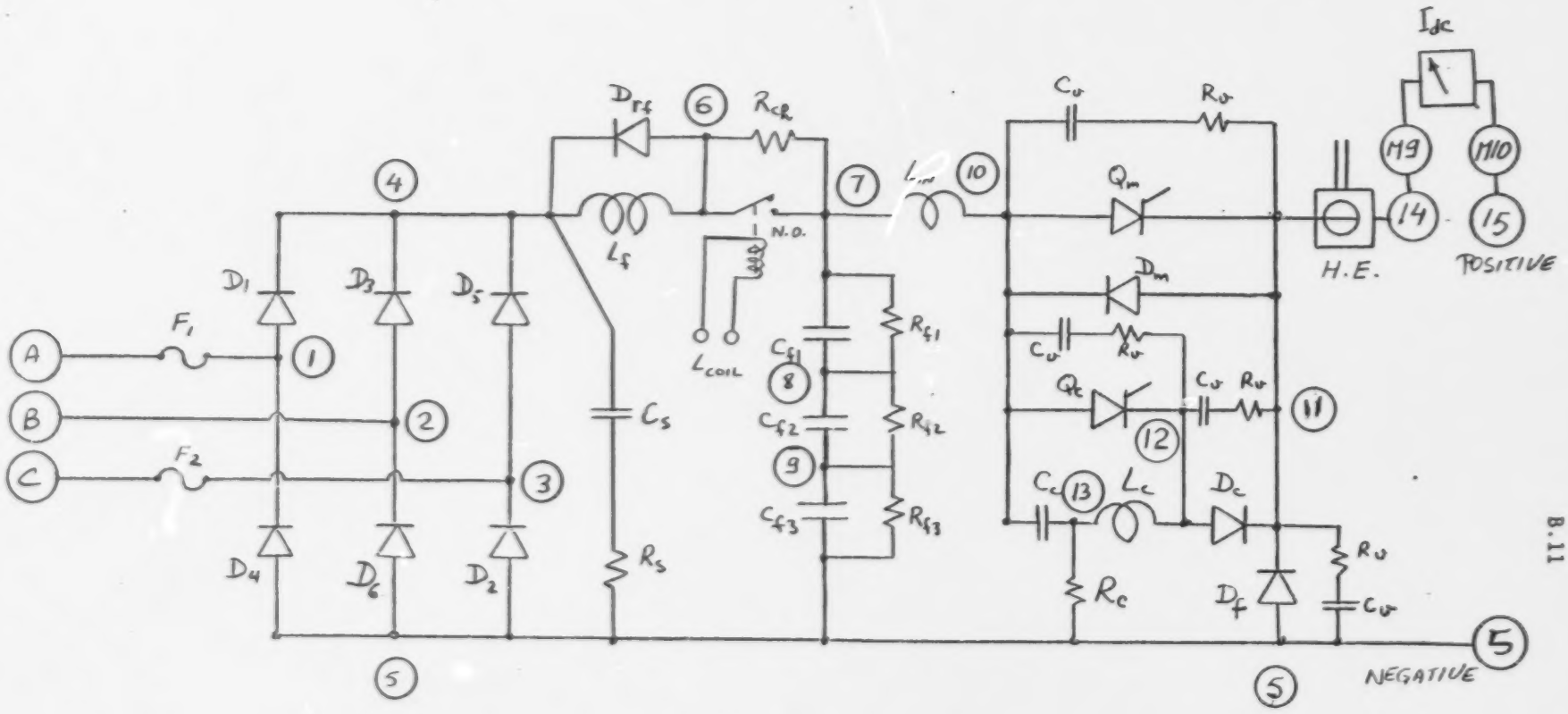


Figure B 5 Detailed power circuit configuration of the rectifier-chopper module for the field winding of the dc motor. The connections between the ciruit components are identified on the hardware by the numbers as shown.

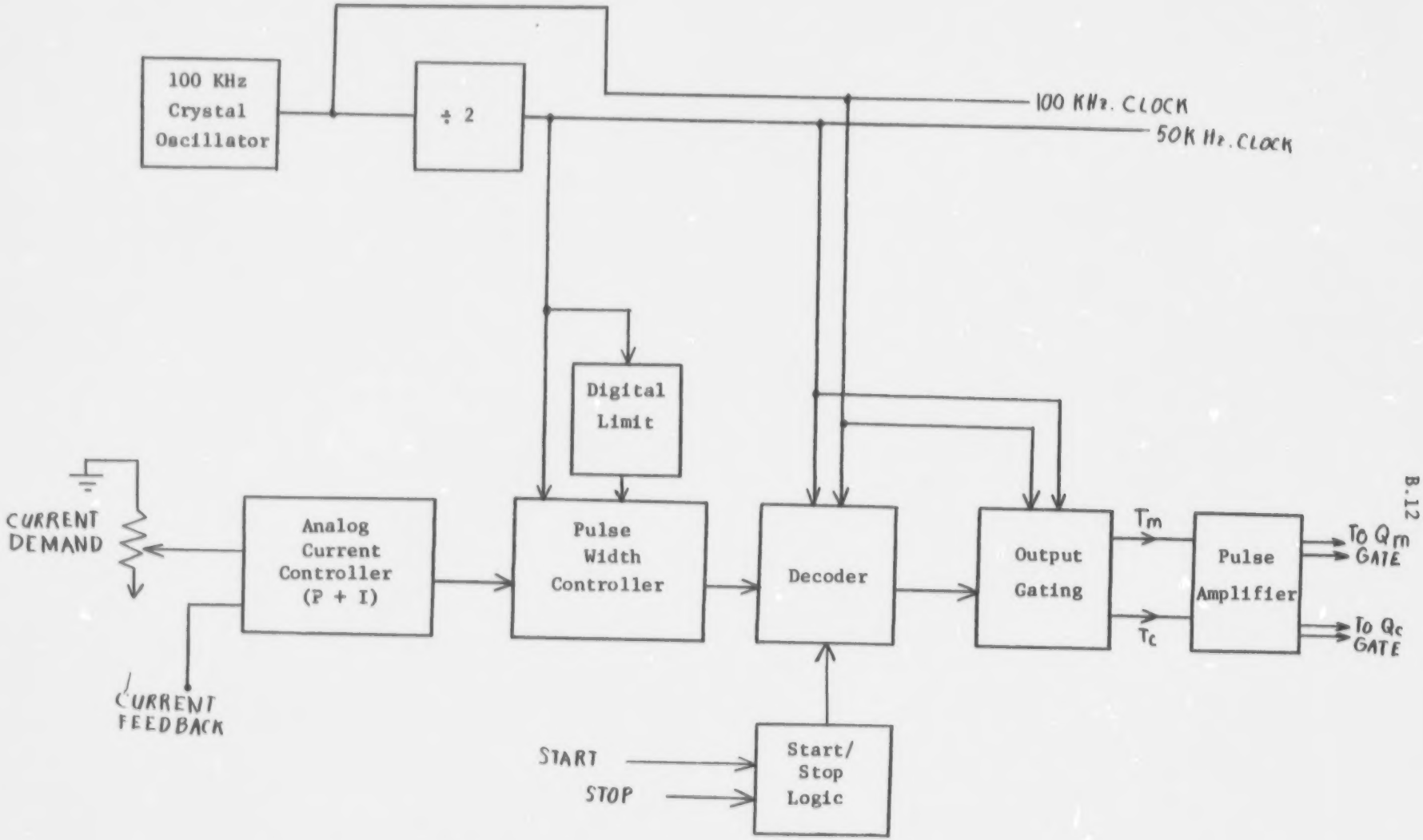


Figure B6 Block diagram of the logic and control circuit for field chopper of Figure B5.

Component	Specifications
Diodes D_1, D_3, D_5	FMC, S34150
Diodes D_2, D_4, D_6	FMC, R34150
Diode D_{rf}, D_f	FMC, DSD 17-11B, 17A, 1100V, 1μs, fast recovery
Diode D_m, D_c	Westinghouse, R6021025EJ, 250A, 1000V, fast recovery
Thyristor Q_m, T_c	Westinghouse T507104064 AQ, 40A, 1000V, 20μs
Inductor L_f	10mH, 10Amp. Hamond, 195J10
Inductors L_{in}, L_c	36 turns on ferrite core, single wire, 300μH
Capacitor C_s	2 x .1μF, 1000VDC
Capacitors C_{f1}, C_{f2}, C_{f3}	900μF, 350VDC, max. surge 400VDC
Capacitor C_c	4 x .5μF, 1000V, 2 in parallel 2 in series
Resistors R_s	10Ω, 50w, Ohmite, non-inductive
Resistor R_c	5KΩ, 12W, 4 in parallel
Resistor R_{ch}	10Ω, 100W, 2 in parallel
Snubber resistors R_v	10Ω, 50W, Ohmite, non-inductive
Snubber capacitors C_v	0.1μF, 1000VDC

Table B2 Component specifications of the loading unit field rectifier-chopper module (Figure B5)

The chopping frequency is fixed at 500 Hz and the pulse width is varied by a current feedback loop using proportional-integral (P.I.) controller. The logic and control circuit for the field chopper is described in detail in the following.

Logic and Control Circuit: Figure B6 shows the block diagram of the logic and control circuit of the field chopper. The chopper operates at a fixed frequency of 500 Hz and uses 'Pulse Width Control' to vary the output voltage. The pulse width is determined by an 'analog current controller' which regulates the output current. A 'digital limit' circuit ensures that the pulse width of the output voltage is limited to a fixed value (adjustable from 90-98%) independent of the current feedback loop. The 'decoder' produces the pulse width signal for gating of the main thyristor, Q_m (Figure B5) and a narrow commutation pulse for gating of the thyristor Q_c (Figure B5). The 'start/stop logic' ensures that the commutation thyristor and the main thyristor are gated in the proper sequence while starting and stopping. The observation of the various blocks in Figure B6 is described below.

(1) Clock Oscillator: A 100 KHz crystal oscillator is used as the reference for the logic. A frequency divider is used to produce an additional 50 KHz clock signal.

(2) Pulse Width Controller: This circuit determines the percentage of time in each 2 ms (500 Hz) period during which the main thyristor Q_m (Figure B5) is conducting.

Figure B7 shows the circuit diagram of the P.W. controller. The circuit consists of an integrator (J) and a comparator (K). The gates A,F and G generate a pulse at 2 ms interval to reset the integrator (J).

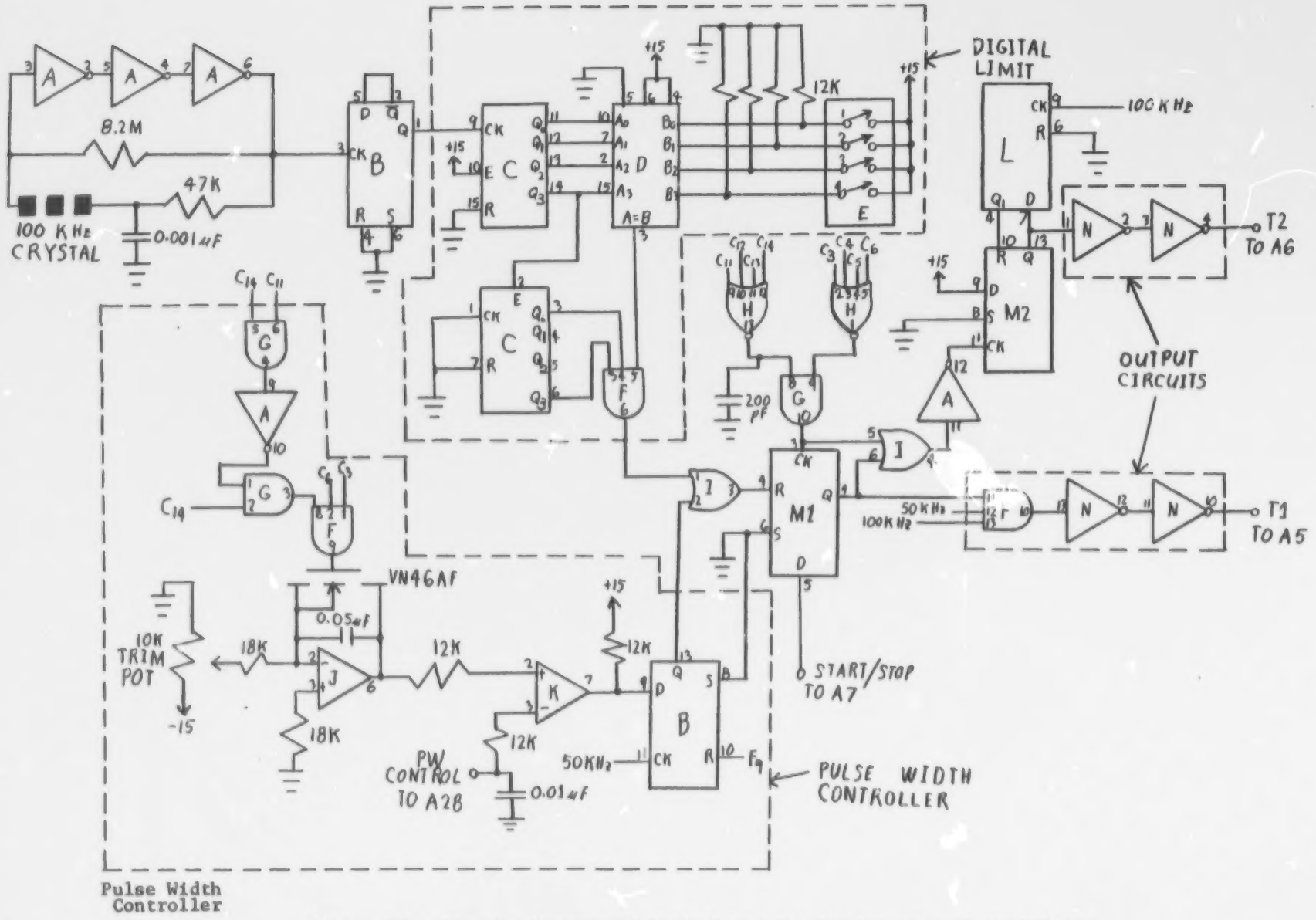


Figure B7 Circuit diagram of logic board B, showing crystal oscillator, digital limit, pulse width controler, decoder and output circuit (c.f. Figure B 6)

The output of the integrator is compared with the Pulse Width control signal, derived from the analog current controller (Figure B6). The output of flip-flop (B) is set to logical one when the ramp output of the integrator exceeds the P.W. control voltage. The flip-flop (B) is reset by the same signal which resets the integrator. Thus, the pulse width of the 500 Hz signal at the output Q (Pin 13) of the flip-flop (B) is determined by the magnitude of the P.W. control voltage. Figure B8 shows the output of the P.W. controller (I_2), the integrator output J6 for a particular value of P.W.control voltage (K_3).

(3) Digital Limit: The function of this block is to limit the pulse width of the gating signal to the main thyristor Q_m (Figure B5). The circuit diagram is shown in Figure B7 and consists of BCD counters (C), digital comparator (D), gate (F) and switch (E). The decade counters are connected in series and count up to one hundred pulses of the 50 KHz clock. This establishes the basic chopping period of 2 ms. The gate F (Pin 6) gives an output when the count of C is between 90 to 98, depending upon the setting of switch E. The on time of the main thyristor Q_m (Figure B5) is terminated either by the P.W. controller (F/F B) or by the digital limit (Gate F). Thus, the P.W. controller cannot increase the on time of main thyristor beyond the time set by digital limit. Figure B8 shows the output (F6) when the limit is set at 90 counts.

(4) Decoder: The decoder produces the basic signal for the on time of main thyristor and a narrow pulse for commutation thyristor at the end of the on time. The circuit shown in Figure B7 consists of flip flops M1, M2 and L and gates G, H, I. The flip flop M1(Pin3) is clocked in when the counters C in the digital limit circuit go to zero at the start of each chopping period. The start/stop signal at pin5 of F/F M1 is set to logical one for start and zero for stop. Therefore, the output Q (Pin1) of F/F M1 is set to one when G10 is set high at the start of chopping period (Figure B8).

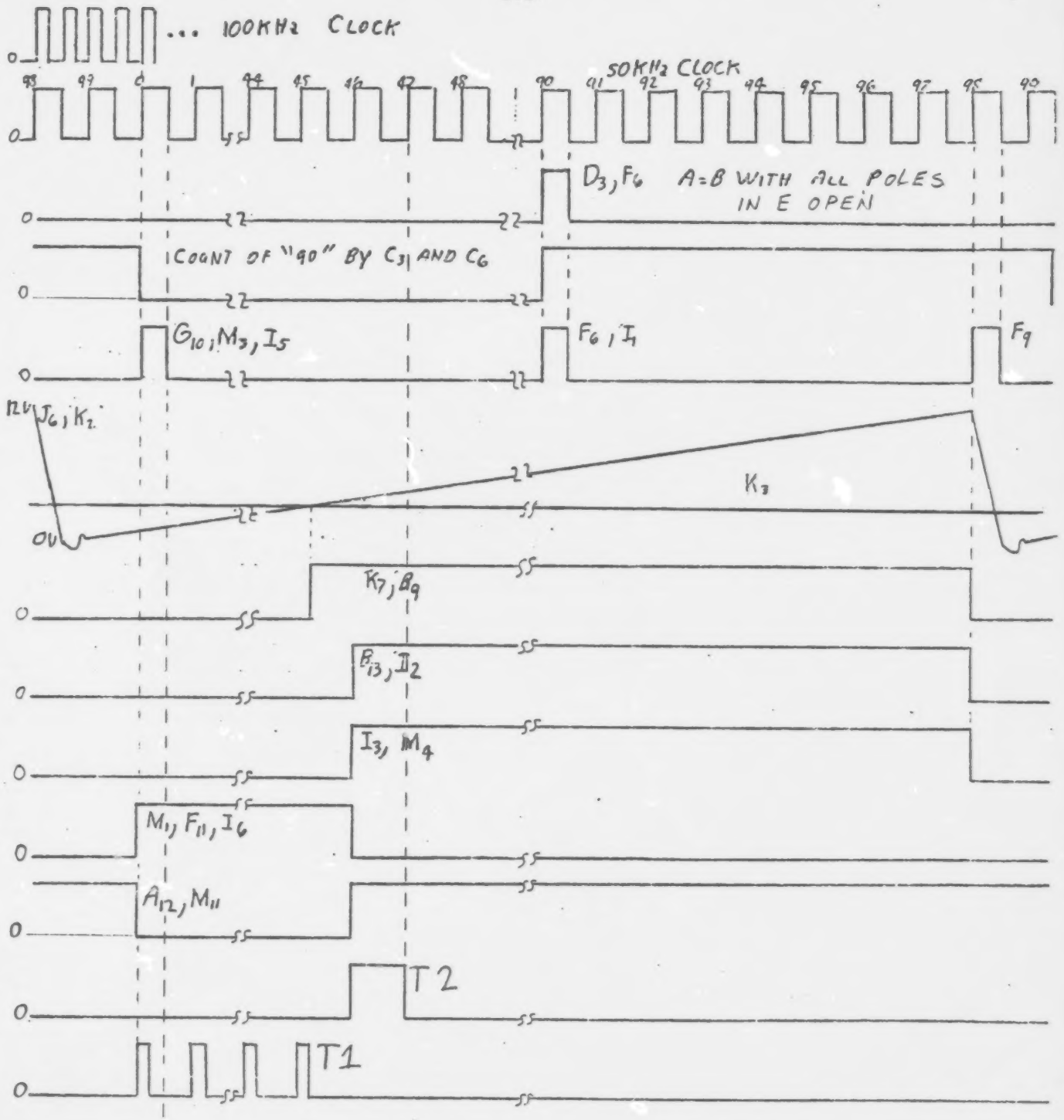


Figure B8 Timing Diagram of logic circuit of Figure B7.

The F/F is reset either by the output of the Pulse Width controller (Pin 13,B) or by the output of the limit circuit (Pin6, F). The reset signals are connected through the OR gate I (Pin 3).

When F/F M1(Pin1) is reset, a clock pulse is applied to F/F M2 (Pin 11). The output Q (Pin 13) of M2 remains high for two cycles and is reset by flip flop L. Thus a 20 μs pulse is produced at the output of M2 (also at T_2) when M1 is reset.

(5) Output Circuits: The output of F/F M1 along with 50 KHz and 100 KHz clocks are connected to an AND gate F to obtain output signal T_1 shown in Figure B8. The H.F. pulses are used to gate the thyristors. The output signal T_2 is obtained directly from F/F M2 through buffer N.

(6) Start/Stop Logic: The circuit for this block is shown in Figure B9. The signals for start and stop are generated by push buttons. A 1 sec. oscillator (R) is used to clock the shift register P. Flip flop S is in reset state ($\overline{Q}$ = 1) when the logic power is turned on and all shift register outputs are zero. When the start button is pressed, F/F S is set, a signal A7 is given to the decoder (Figure B7 , F/F M1) to generate the gating signals T_1 and T_2. Simultaneously, a shift right command appears at shift register P through gate Q. Thus the outputs of shift register P go to one from Pin 15 (top most) to 12 (bottom most in Figure B9 . Therefore the following starting sequence is generated.

(a) Signal A6 (or T_2 in Figure B7 is connected to the output A4 and the gate signals to commutation thyristor are started.

(b) The VMOS switch is gated to provide signal for relay logic which shorts the charging resistor (in Figure B5).

(c) Signal A5 (or T_1 in Figure B7) is connected to the output A3 and the gate signals to the main thyristor are started.

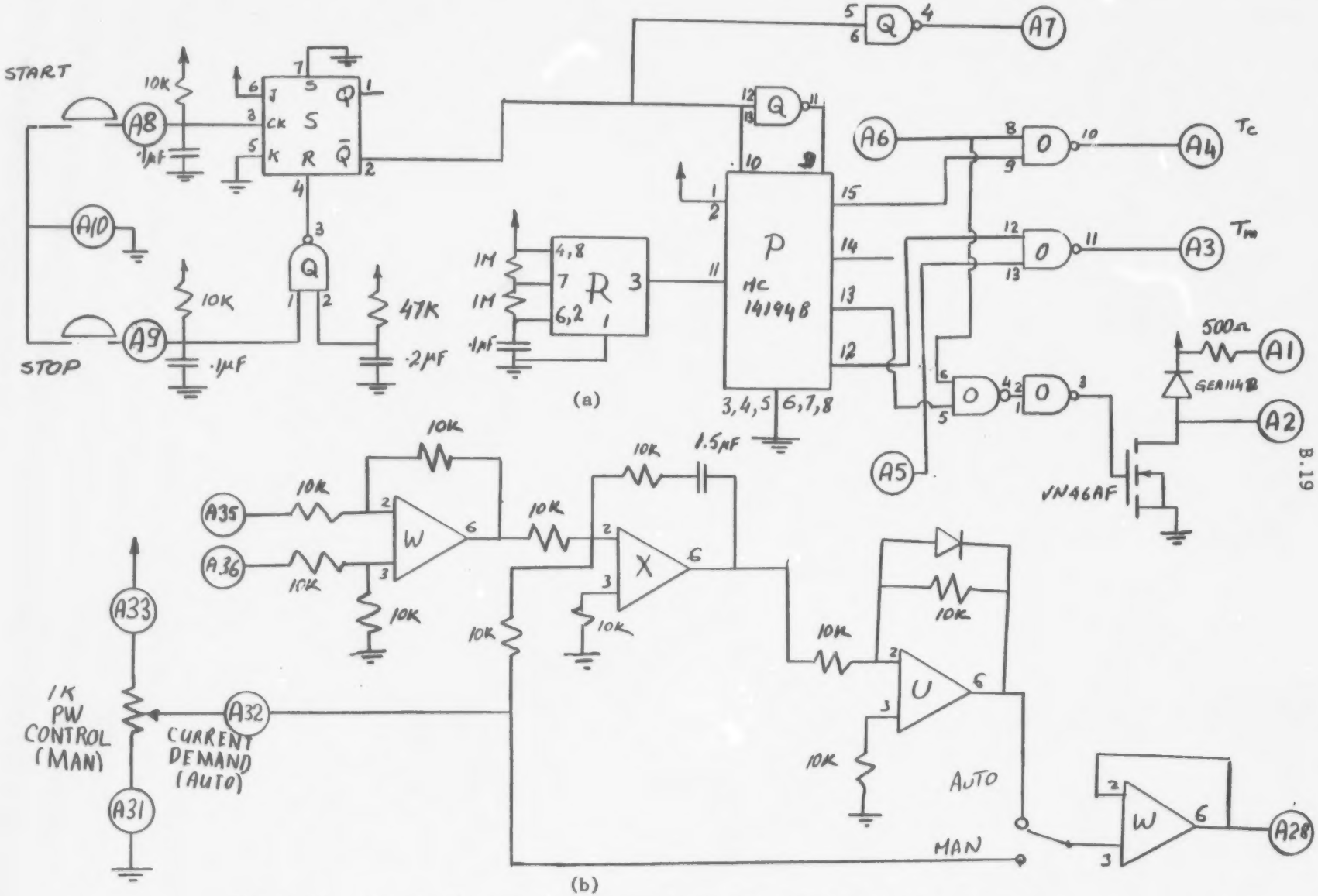


Figure B9 Circuit diagram of (a) start/stop logic and (b) analog current controller. These circuits are assembled on logic board A.

When the stop button is pressed flip flop S is reset and signal at A7 goes to zero. Thus, the next cycle of gating signals T_1 and T_2 is terminated. A shift left command now appears at the shift register P. The sequence (a), (b), (c) given above is now reversed. Thus, the main thyristor gating is turned off, followed by the VMOS switch. The commutation thyristor is gated last to ensure that main thyristor is off at the end of the sequence.

(8) Analog Current Controller: This circuit shown in Figure B 9 generates the input signal for the pulse width controller (Figure B 7, A28) The current demand reference is set by a potentiometer. The current feedback signal derived from Hall Effect transducer (Figure B 5) is connected through a differential amplifier, W. The reference and the feedback signal are fed to a proportional — Integral (P.I.) controller, X. The output of the P.I. controller is connected to output when the switch is in AUTO position. In MAN position the current demand reference is directly connected to the output, A 28 and can be used to control the pulse width of the chopper.

Layout of the Logic and Control Circuit

The logic and control circuit of the chopper is assembled on two boards shown in Figure B 10. The terminal connections are connected through strip L and the indicating instruments are connected on panel M. The detailed wiring diagrams for the interconnections between the various sub-assemblies of the logic are given at the end of this section. The connections on the logic board A and B are designated with prefix A and brought out on the logic strip, (prefix L). The connections to the front panel are designated with prefix M.

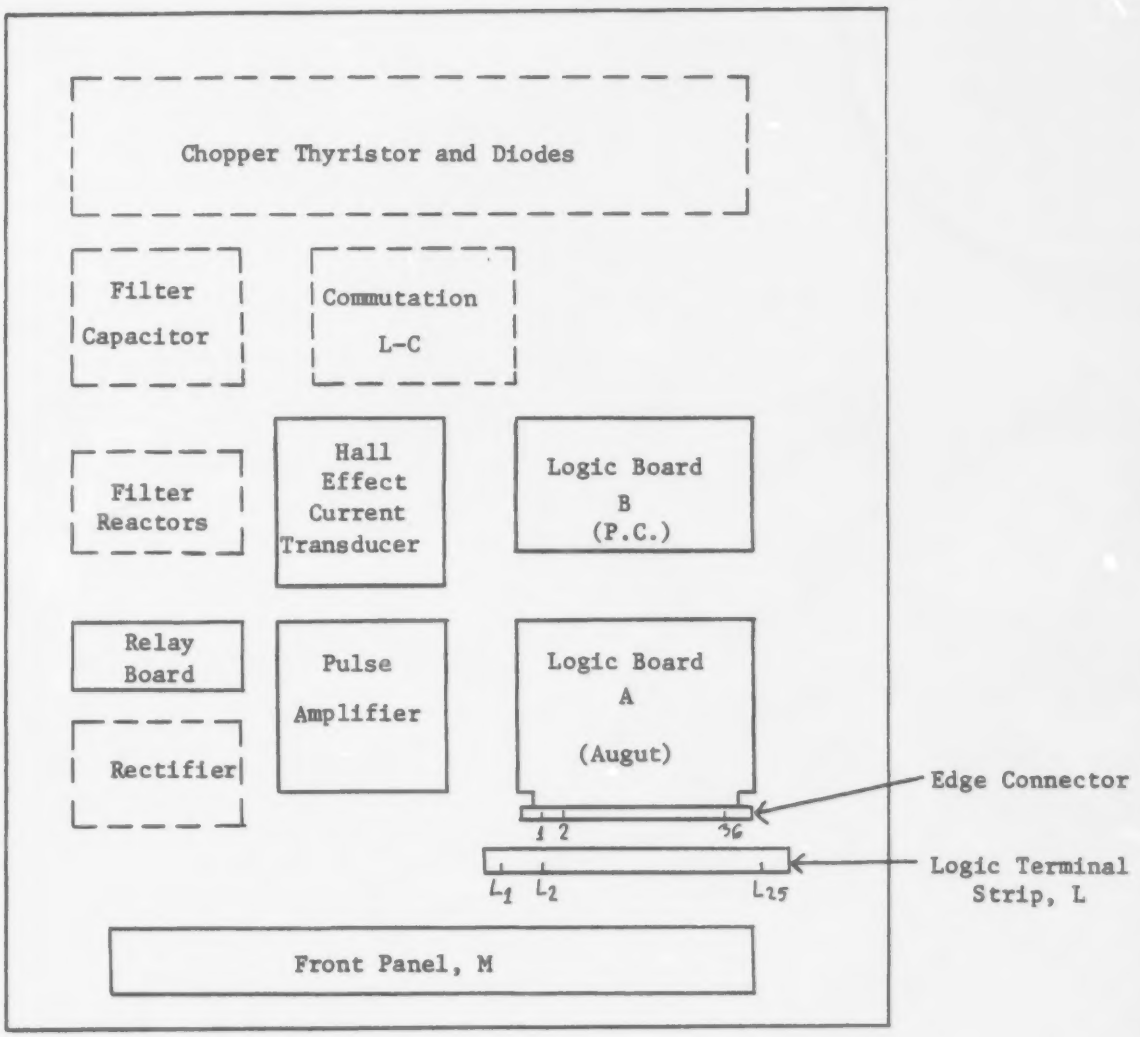
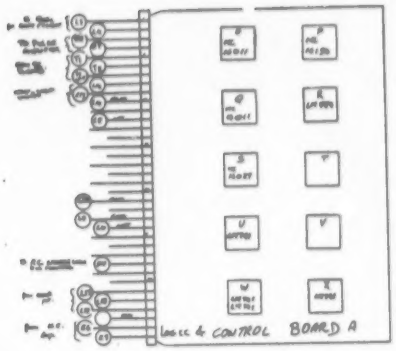


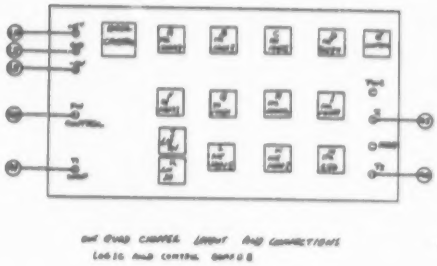
Figure B10 Layout of components of the logic and control circuit and power circuit of the rectifier chopper module.

LIST OF DETAILED DRAWINGS

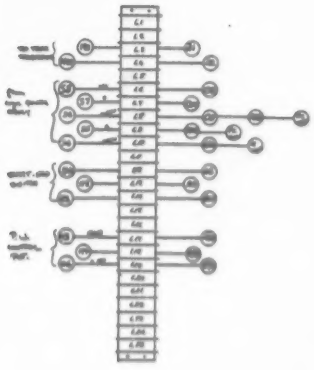
D1	Layout of Logic and Control Board A
D2	Layout of Logic and Control Board B
D3	Connections at Logic Terminal Strip
D4	Pulse Amplifier Connections
D5	Pulse Amplifier Schematic and Board Layout
D6	Front View of the Front Panel
D7	Front Panel Wiring
D8	Start and Light Circuits
D9	Description of I.C. Chips



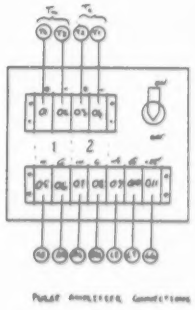
D1 Layout of Logic and Control Board A



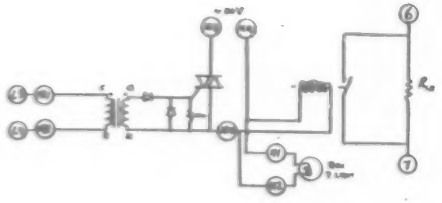
D2 Layout of Logic and Control Board B



D3 Connections at Logic Terminal Strip

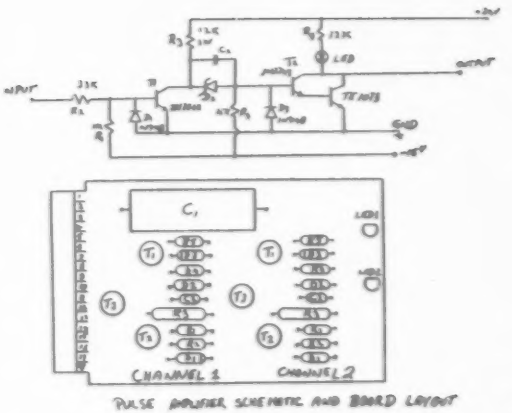


D4 Pulse Amplifier Connections



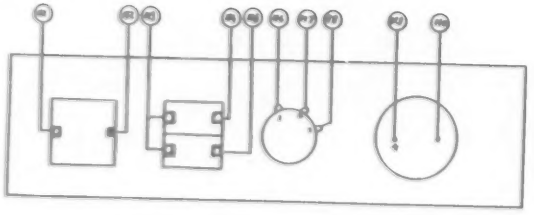
START AND LIGHT CIRCUITS

D8 Start and Light Circuits



PULSE AMPLIFIER SCHEMATIC AND BOARD LAYOUT

D5 Pulse Amplifier Schematic and Board Layout



FRONT PANEL WIRING

D7 Front Panel Wiring

FRONT VIEW OF THE FRONT PANEL

D6 Front View of the Front Panel

A - 4049 - INVERTING BUFFER

B - 4013 - TYPE D FLIP-FLOP

C - 4518 - BCD UP COUNTER

D - 4585 - 4-BIT MAGNITUDE COMPARATOR

E - BINARY SWITCHES

F - 4073 - 3-INPUT AND GATE

G - 4081 - 2-INPUT AND GATE

H - 4002 - 4-INPUT NOR GATE

I - 4071 - 2-INPUT OR GATE

U,W,J - 741 - OPERATIONAL AMPLIFIER

K - 311 - COMAPRATOR

L - 4015 - 4-BIT STATIC SHIFT REGISTER

M - 4013 - TYPE D FLIP-FLOP

N - 680 - INVERTING BUFFER

Q,O - 4011 - 2-INPUT NAND GATE

P - 4194 - 4-BIT SHIFT REGISTER

R - 555 - TIMER

S - 4027 - JK FLIP-FLOP

D9 DESCRIPTION OF I.C. CHIPS

APPENDIX C

CHOPPER CURRENT SOURCE UNIT

APPENDIX C

CHOPPER CURRENT SOURCE UNIT

C1 Introduction

The required power for the current source inverters is supplied by a chopper current source whose input is connected to a dc power supply. The chopper is capable of both accepting and supplying a dc power from/to one or more current source inverters. The specifications and the detailed description of a 2-quadrant chopper unit fulfilling the above requirements are as follows.

C2 Specifications

Fig. C1 demonstrates the block diagram of the required 2-quadrant chopper current source unit. This chopper is designed to operate from a nominal 600 VDC bus and with a nominal input current of $\pm$ 400 ADC. It can produce an output unidirectional current up to 400 ADC while the output voltage can be controlled from 0 to 600 VDC in both positive and negative directions. In this manner, the chopper can supply one or more current source inverters in both motoring and braking regions. The unit is provided with meters for both input and output voltages and currents. This unit always operates at a fixed frequency (controlled by an oscillator) and no frequency modulation is necessary at any point of operation on the traction torque/speed curve. The on-time of the chopper can be measured with a counter and the chopper can be operated in manual (on time control) as well as automatic current regulation mode. Some of the additional features of the design are:

(i) All the components are water cooled such that the chopper losses can be measured with water flow and temperature measurements.

(ii) Small signal logic protection is provided for lower limit of dc input voltage (avoids loss of commutation), higher limit of dc input voltages (avoids over-voltage across solid state power components) and overcurrent in the output (if regulating feedback loop has a malfunction).

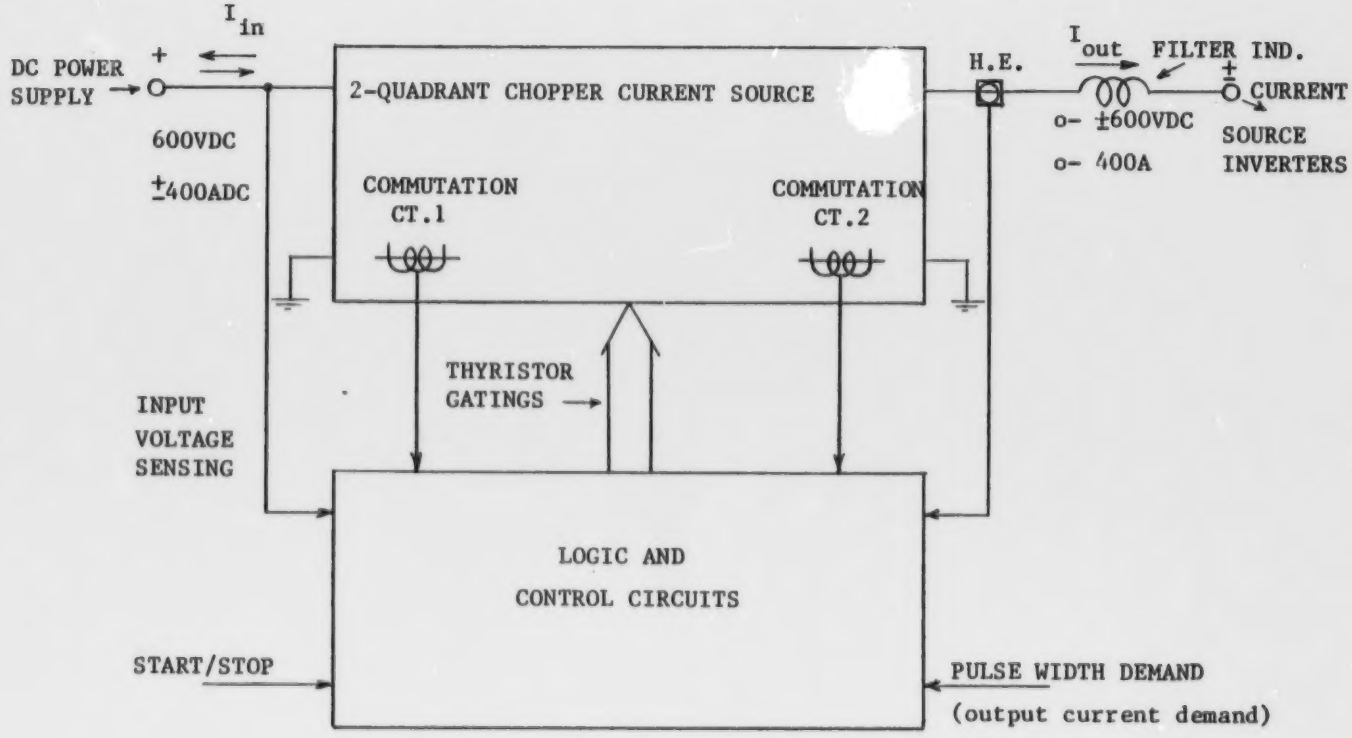


Fig. C1 Block diagram of 600VDC, 400ADC, 2-quadrant chopper current source

C3 Detailed System Description

The current commutated two quadrant chopper described in this section is used to supply adjustable dc current to the inverter. The chopper circuit is capable of providing positive or negative output voltage and positive (unidirectional) output current. A large filter inductor is connected in series with the output to provide ripple free current. A feedback control system automatically adjusts the output voltage of the chopper to provide constant output current.

The power circuit configuration and the logic and control circuits for the chopper are described in this section.

C3.1 Power Circuit Configuration: Fig. C2 shows the basic power circuit of the chopper. The thyristors Q_1 and Q_2 are the main power switches and diodes D_{f1} and D_{f2} are the freewheeling diodes. The thyristor Q_1 is turned off by a commutation circuit consisting of Q_{11}, D_{11}, D_1, L_1 and C_1. The commutation process is initiated by gating thyristor Q_{11}. Similarly, thyristor Q_2 is turned off by the commutation circuit consisting of Q_{22}, D_{22}, D_2, L_2 and C_2. Inductor L_f is connected in series with the output to filter the output current. The resistors R_1 and R_2 (Fig. C2) provide the initial charge on the commutation capacitors C_1 and C_2 respectively. Fig. C3 shows the detailed power circuit diagram of the chopper. The snubber networks (Rv, Cv) are connected in parallel across the thyristors and diodes to limit the dv/dt. The numbers in Fig. C3 refer to physical connections between components and correspond to the labels on the wires in the hardware.

In Figs. C2 and C3, the current transformers CT.1 and CT.2 are connected in series with the commutation capacitors C_1 and C_2 respectively. Fig. C4 shows the details of the current transformer secondary circuit which sends a low level signal to the overcurrent protector in the logic circuit.

The output current of the chopper is monitored by a Hall Effect current transducer shown in Figs. C2 and C3. The output signal of this transducer is connected to the logic circuit for the current regulation and overcurrent protection. Fig. C5

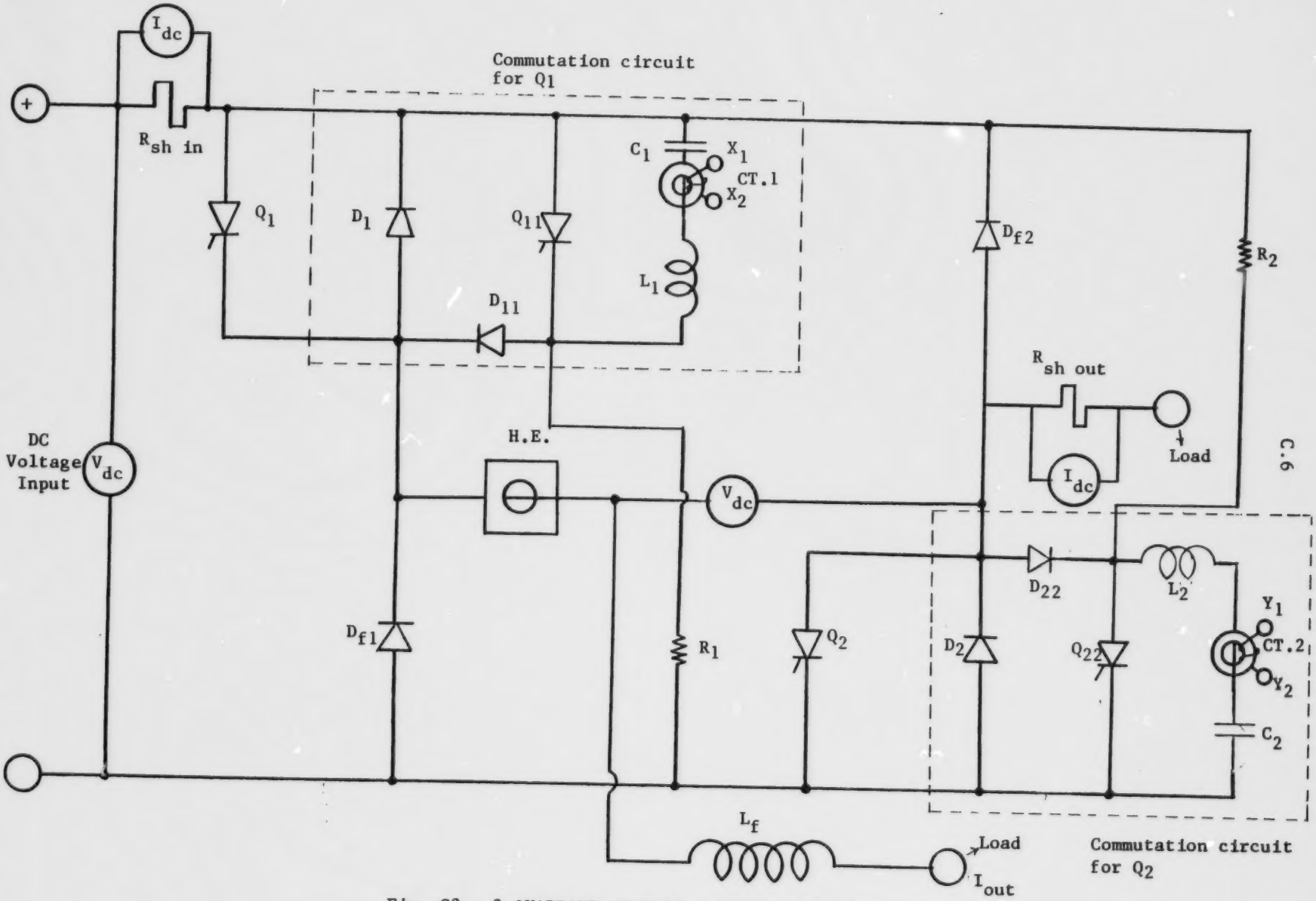


Fig. C2 2-QUADRANT CHOPPER - POWER CIRCUIT

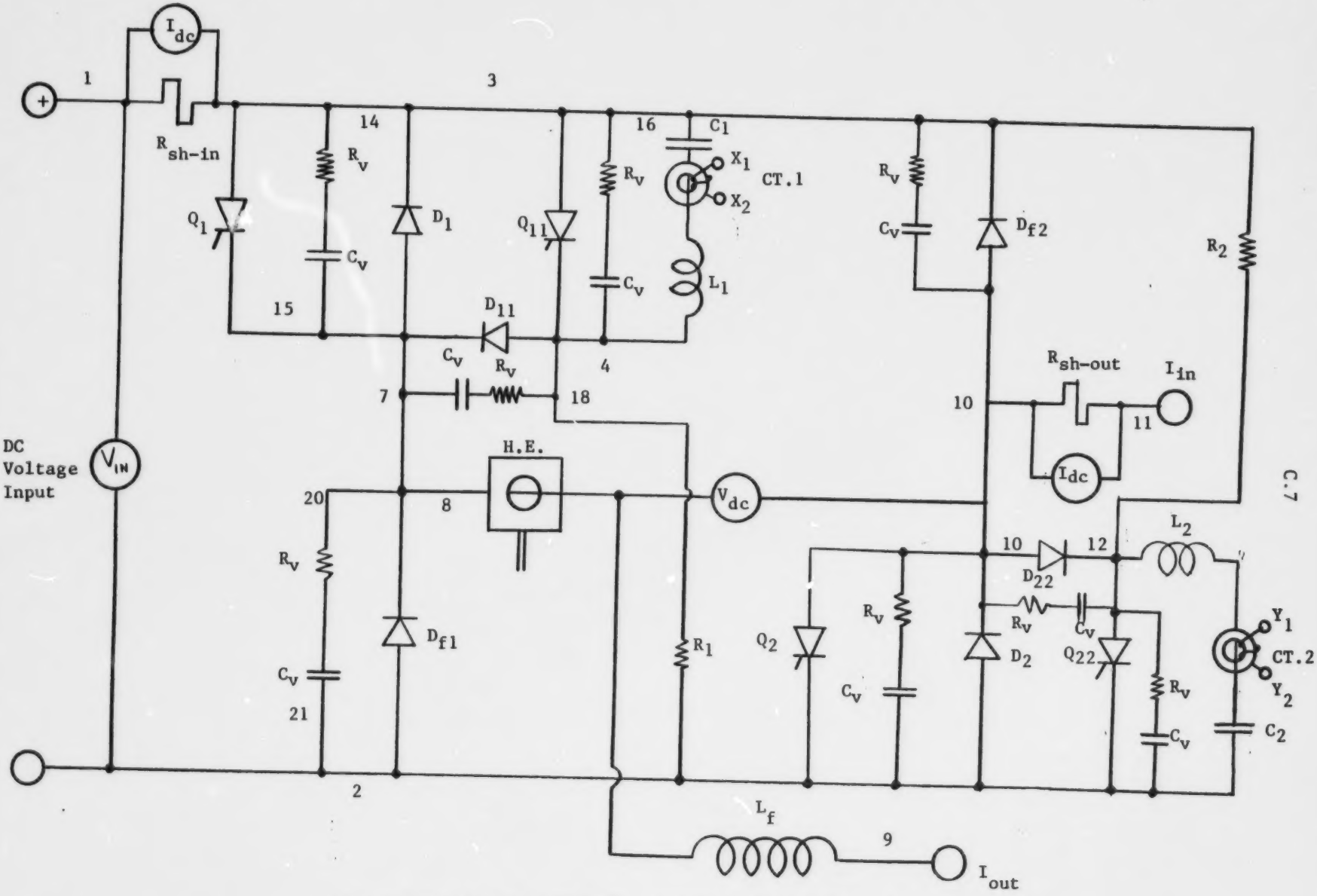
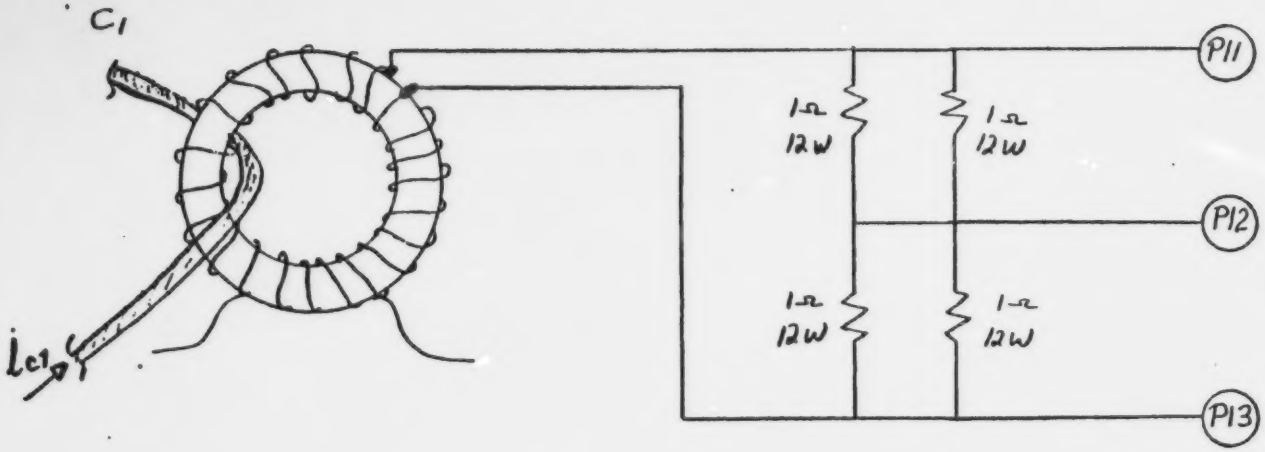
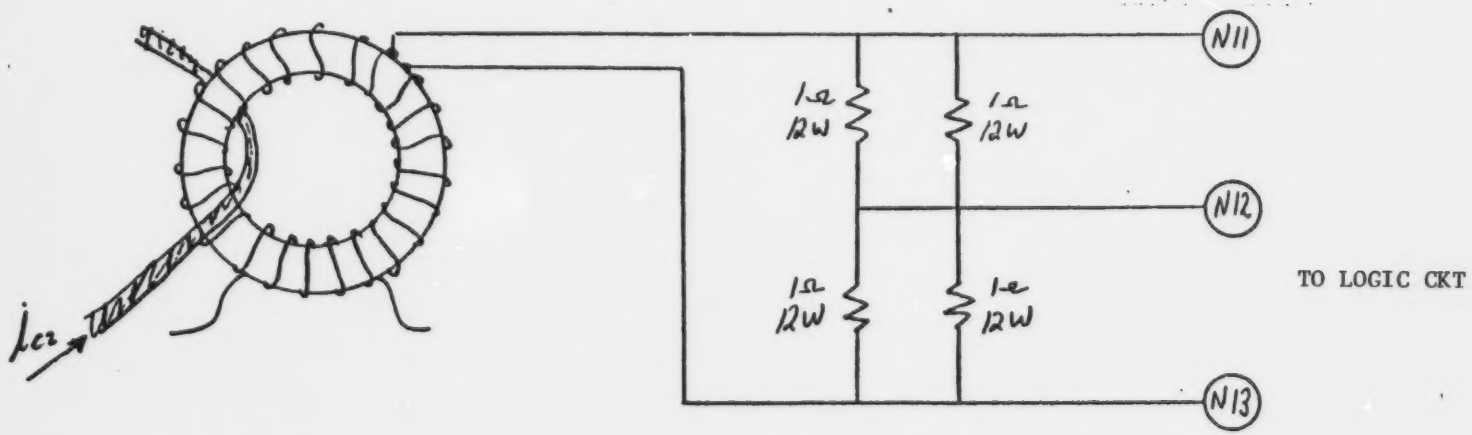


Fig. C3 2 QUADRANT CHOPPER - DETAILED POWER CIRCUIT

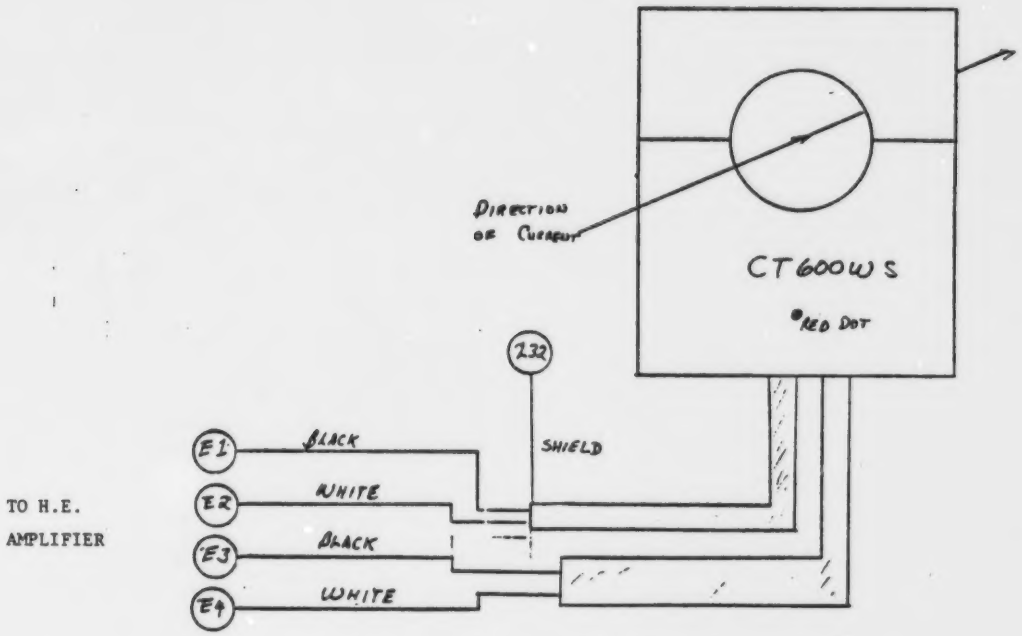


(a) TOP SHELF COMMUTATION CURRENT SENSING (CAPACITOR C1)

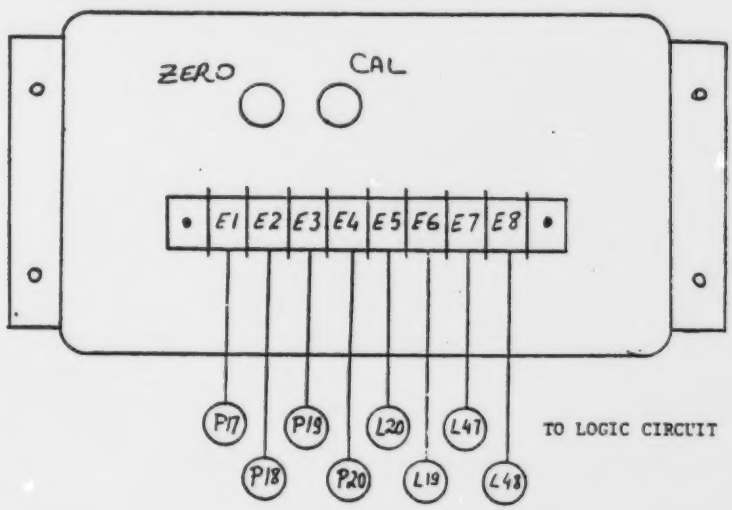


(b) BOTTOM SHELF COMMUTATION CURRENT SENSING (CAPACITOR C2)

FIG. C4 CONNECTIONS OF THE CURRENT TRANSFORMERS TO THE LOGIC AND CONTROL CIRCUIT.



(a) HALL EFFECT CURRENT SENSING



(b) HALL EFFECT AMPLIFIER CONNECTIONS

FIG. C5 SENSING CIRCUITS FOR OUTPUT CURRENT USING HALL EFFECT TRANSDUCER.

shows the details of the connections of Hall Effect current transducer and amplifier. Table C1 gives the specifications of the components employed in building the circuit of Fig. C3.

Component	Specifications
Thyristors Q_1,Q_{11},Q_2,Q_{22}	Westcode, R220AH12FLJμ5, 600A, 1200V, 12μS
Diodes D_1,D_{11},D_{f1},D_2,D_{22},D_{f2}	GE, A396PB31X, 250A, 1000A
Capacitors C_1,C_2	GE, 341X506FC, 1 μF, 550 VAC, 18 KHz, each 10 in parallel
Inductors L_1,L_2	7 μH, 400A
Resistors R_1, R_2	5000Ω, 12W, each 3 in series
H.E. Current sensor H.E. Amplifier	OSI, CT 600LS, 600A OSI, CTA101, ±50mV, ±10V, 100mA, 115 VAC
Current transformer CT.1, CT.2	100:1, 5A wire
Shunts R_{shin}, R_{shout}	500A, 50mV
Voltmeter V_{in} Voltmeter V_{out} Ammeter I_{in} Ammeter I_{out}	GE, 0-750 VDC GE, 750-0-750 VDC GE, 600-0-600 ADC GE, 0-600 ADC
Inductor L_f	4 in series of 45 turns, in diam. 14"
Snubber resistor R_v	2 of 10Ω, 100W in parallel, Ohmite, non-inductive
Snubber capacitor C_v	0.25 μF, 100 VDC

TABLE C1 SPECIFICATIONS OF COMPONENTS IN THE CHOPPER POWER CIRCUIT (FIG. C3).

C3.2 Logic and Control Circuits

The block diagram of Fig. C6 displays the logic system of a 2-quadrant chopper. The chopper unit controlled by this logic system functions as a current source feeding the two current source inverters in Fig. 1.1. The required output dc current of the chopper is adjusted by the "Pulse Width Demand" signal as shown in Fig. C.6. The "Hall Effect Current Feedback" signal is compared with the demanded signal and the output of the "Analog P.W. Controller" determines the output frequency of the "Voltage Controlled Oscillator". This frequency adjusts the periods of thyristor gating signals such that the resultant output current of chopper becomes the same as the desired value. The other blocks of Fig. C.6 serve as protective circuits which shut off the gating of the chopper thyristors in case of any malfunctions. In this sub-section the following parts constituting the logic system of Fig. C.6 are described and their functions explained.

1. Analog Pulth Width Controller/Instantaneous Over Current Detector.
2. Voltage Controlled Oscillator.
3. 2-Quadrant Chopper Logic/High Frequency Carrier.
4. Commutation Over Current Detector.
5. Over/Under Voltage Signals.
6. Sequential Start/Stop Logic and Fault Protection Decoding.
7. Pulse Amplifier.
8. Logic Layout and Connections.

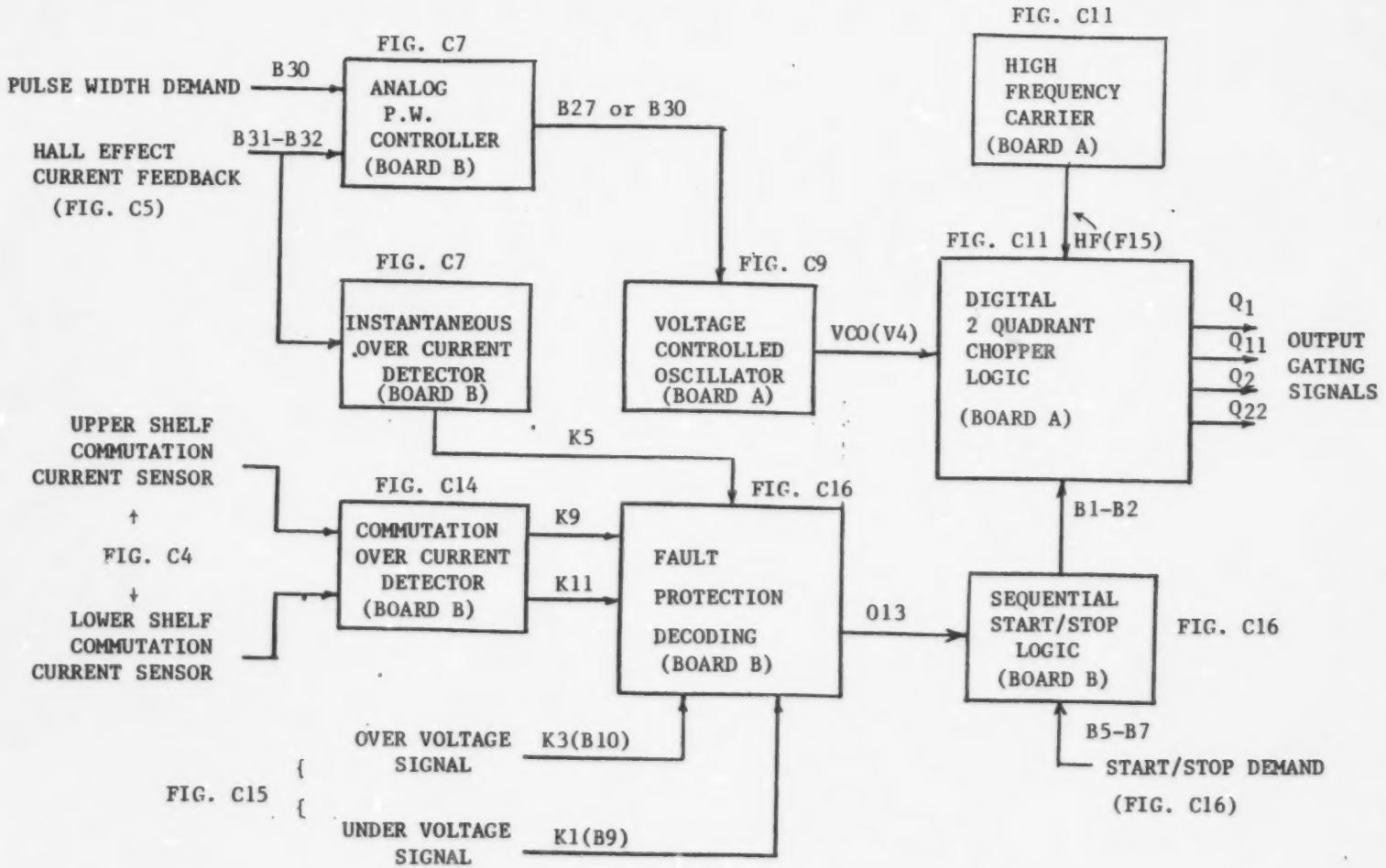


FIG. C6 2 QUADRANT CHOPPER LOGIC SYSTEM - BLOCK DIAGRAM

C3.2.1 Analog Pulth Width Controller/Instantaneous Over Current Detector

Fig. C7 shows the logic circuit required for performing these two functions. The IC chips of this circuit are located on Board B. The layout and IC code numbers of Board B are given in Fig. C8. The output signal of Hall Effect transducer after being amplified is connected across terminals 31 and 32 of Fig. C7 which then constitutes the current feedback signal. The voltage across the 10K resistor connected to terminals 31 and 32 is proportional to the chopper output current. The negative of this voltage appears at P_b6 which then becomes the inputs to the pulse width controller and the over current detector. In the former circuit this input after passing through the low pass filter P_t gives an output at P_t6. The desired chopper output current is adjusted by changing the potentiometer connected to terminal 30. The signal at P_t6 and the reference signal at terminal 30 are the inputs to proportional-integral controller Q_6 the output of which is then added to a negative voltage connected to Q_t2. The final output at Q_t6 is the input to a controlled oscillator (VCO), Fig. C9, which determines the required pulse width of chopper thyristor gating signals.

The signals at P_b6 is also the input to low pass filter R_b. The output signal at R_b6 yields a "Low" signal at output of Comparator R_t, K5, as long as it is smaller than the reference voltage at R_t3. In the event of an excessive chopper output current K5 becomes "High" thus shutting off the chopper thyristor gating signals, Figs. C16, C11.

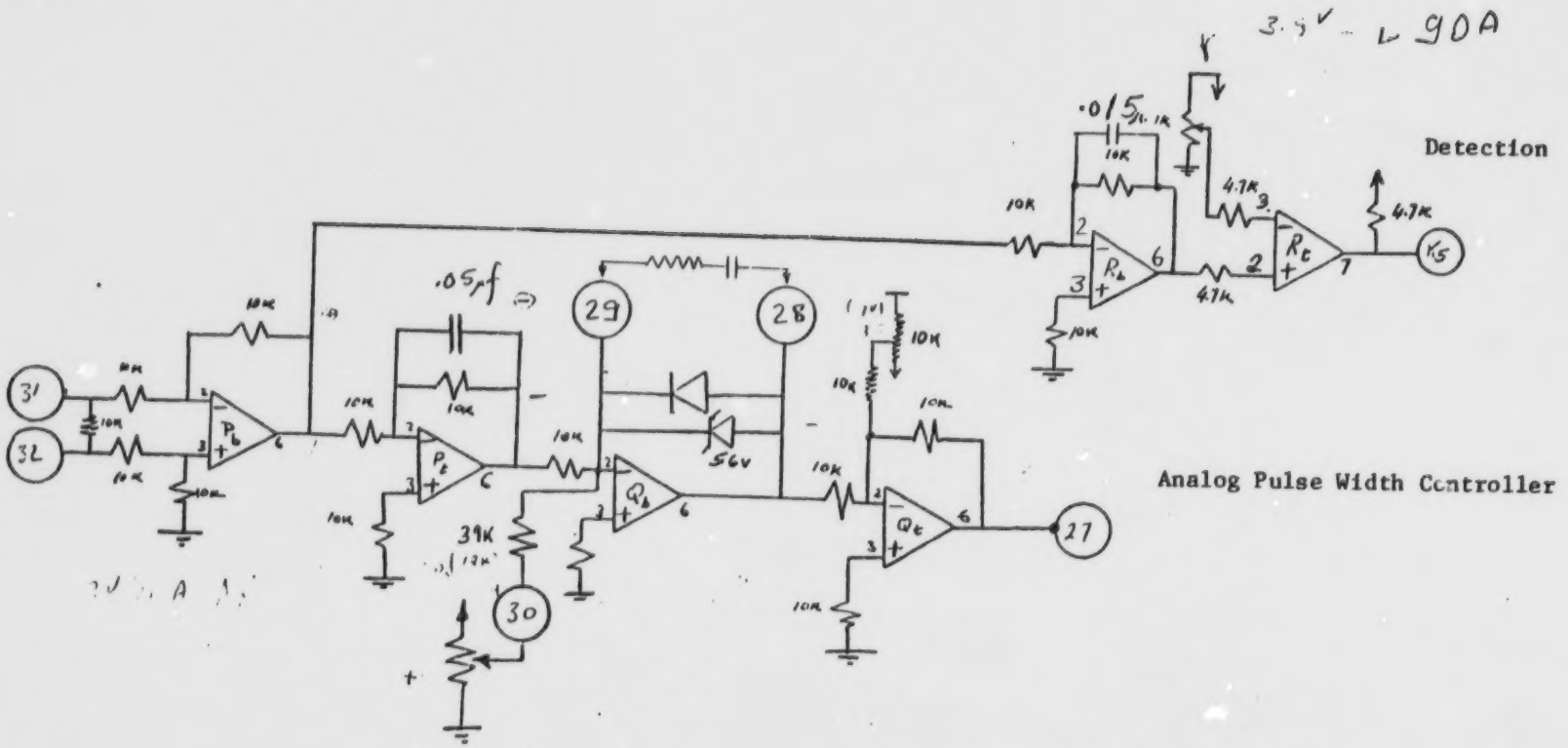


Fig. C7 ANALOG PULSE WIDTH CONTROLLER AND OVER CURRENT DETECTION (BOARD B)

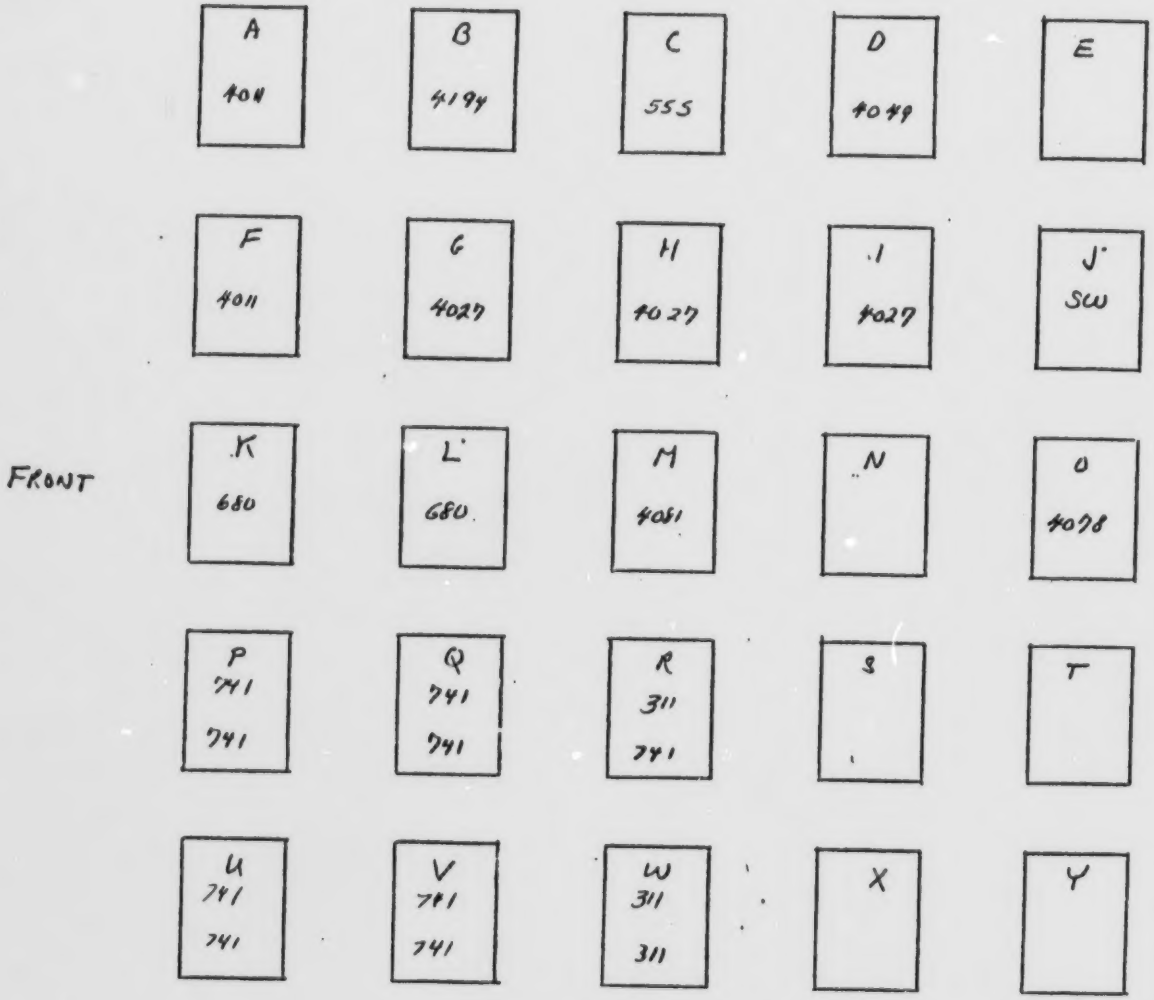


Fig. C8 ANALOG P.W. CONTROLLER AND PROTECTION CIRCUITS - BOARD B

A Quad 2-Input NAND Gate
B 4-Bit Universal Shift Register
C Timer
D Hex Inverter/Buffer
E
F Same as A
G Dual JK Flip-Flop
H Dual JK Flip-Flop
I Dual JK Flip-Flop
J Switch
K Buffer
L Buffer
M Quad 2-Input AND Gate
N
O 8-Input NOR Gate
P OP Amp (2)
Q OP Amp (2)
R Comparator - OP Amp
S
T
U OP Amp (2)
V OP Amp (2)
W Comparator (2)
X
Y

C3.2.2 Voltage Controlled Oscillator

The output of the pulse width controller of Fig. C7 is the input to the circuit of Fig. C9. The IC chips of Fig. C9 are located on Board A. The layout and IC code numbers of Board A are shown in Fig. C10. The positive input signal at terminal 10 of Fig. C9 after passing through voltage follower U is the input to the VCO whose output frequency is proportional to the level of the input signal. The two 10K resistors in conjunction with the corresponding diodes connected to the non-inverting input of voltage follower U adjusts the range of VCO output frequency.

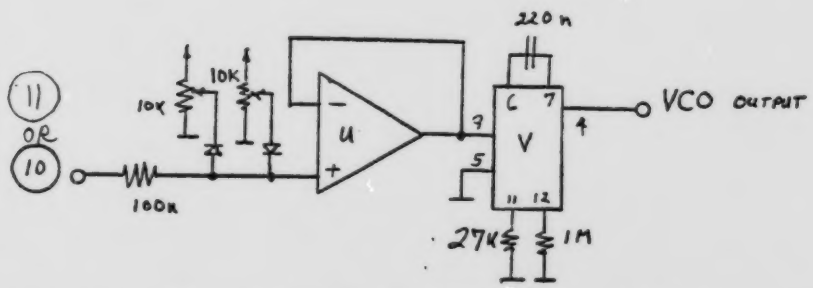
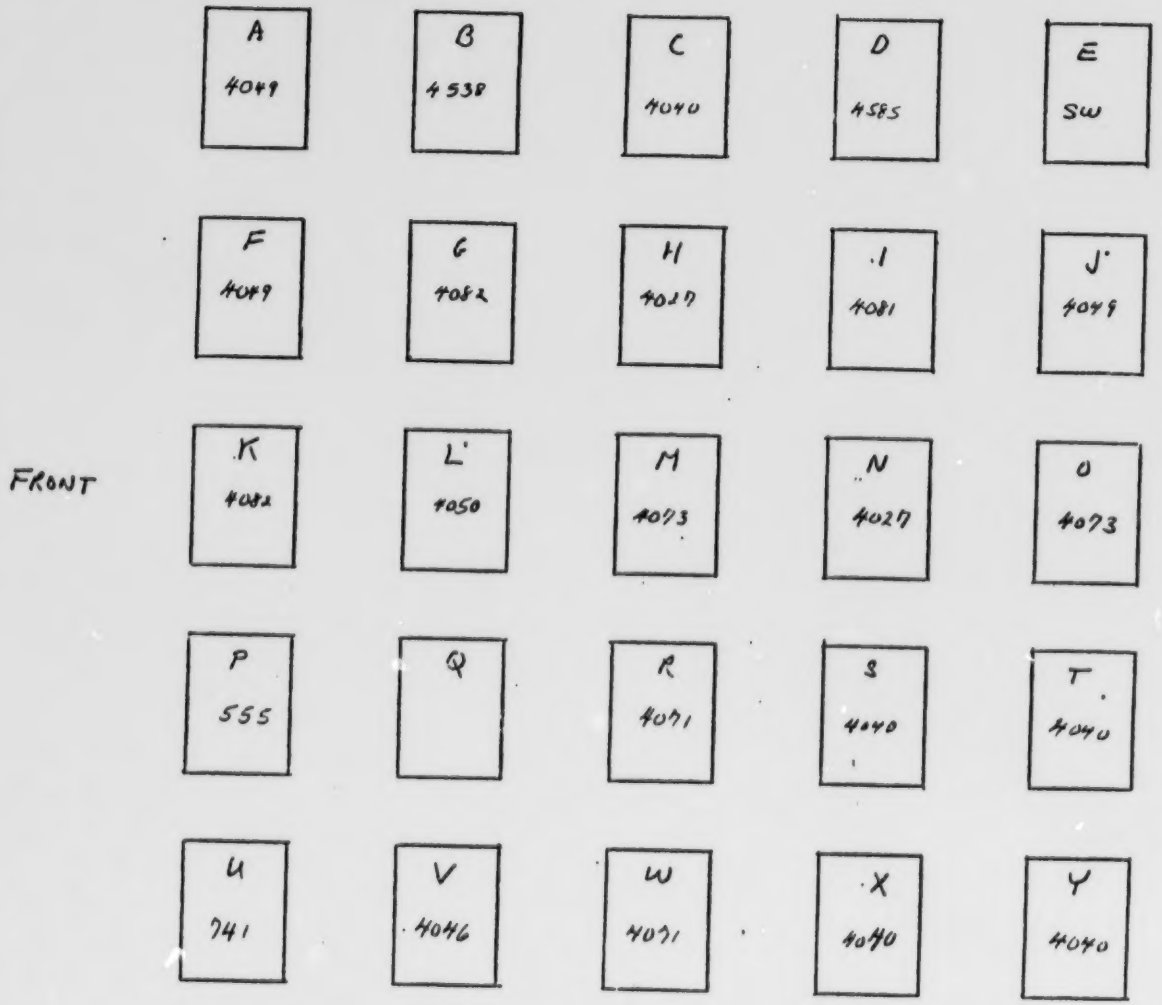


FIG. C9 VOLTAGE CONTROLLED OSCILLATOR (BOARD A)



A Hex Inverter/Buffer
B Dual Precision Monostable
C 12-Bit Binary Counter
D 4-Bit Magnitude Comparator
E Switch
F Same as A
G Dual 4-Input AND Gate
H Dual JK Flip-Flop
I Quad 2-Input AND Gate
J Same as A
K Quad 2-Input NAND Gate
L Hex Buffer
M Triple 3-Input AND Gate
N Same as H
O Same as M
P Timer
Q
R Quad 2-Input OR Gate
S Same as C
T Same as C
U OP Amp
V Phased-Locked Loop
W Same as R
X,Y Same as C

Fig. C10 2 QUADRANT CHOPPER LOGIC LAYOUT - BOARD A

C3.2.3 2-Quadrant Chopper Logic/High Frequency Carrier

The logic circuit shown in Fig. C11 is used in gating the thyristors of a 2-quadrant chopper whose power circuit was given in Fig. C2. The operation of the chopper gated by the circuit of Fig. C11 is according to pulse width modulation method where the chopping frequency is kept constant while the width of the output voltage pulses can be varied. Depending on the frequency of pulses received from VCO the resultant thyristor gating signals generated by the logic circuit of Fig. C11 can result in two modes of chopper operation: (a) motoring; (b) braking. Figs. C12 - C13 show the waveforms of signals at different points of Fig. C11 and for the above mentioned chopper two modes of operation. The following description in conjunction with the timing diagram of Fig. C12 explains the operation of the 2-quadrant chopper logic circuit of Fig. C11.

The 12-bit binary counter C receives its clock pulses from a 1MHz oscillator. The signals appearing at G13 have a frequency almost equal to 1KHz (992 Hz). Dip switch (E) in conjunction with magnitude comparator (D) provides the necessary commutation time for a complete thyristor turn-off. The output of monostable (B) consists of narrow pulses with the same frequency as those at G13 (≈ 1KHz). These signals are shown by Reset (A) waveforms in Fig. C12. The complement of signals (A) drive one of the JK flip-flops in H. This flip-flop is reset by Delay Pulses (B) so that the pulses appearing at H1 have widths equal to the delay time between pulses (A) and (B) and a frequency equal to that of clock pulses at H3. The way signals (E) and (F) appear at I3 and I4 is

quite clear from the corresponding waveforms in Fig. C12 and the logic circuit of Fig. C11. The widths and frequency of these signals are respectively equal to and half of those of signals (C) at H1. The generation of signals (I), (J), (K) and (L) also are clear from Figs. C11 and C12. These signals are as narrow as Reset (A) signals at B6 while their frequency is ¼ of signals (A). The 12-bit binary counters T, S, Y and X receive their clock pulses from OR gates W. These counters all operate on the same principle. Considering counter T it is noticed that T14 goes "High" after arriving 512 of VCO pulses at W1. As soon as T14 goes "High" the pulses of VCO have no more effect on counter T so that T14 stays "High" till the time it is reset by signal (I). Depending on the frequency of VCO output signals the interval during which T14 stays "High" in each cycle may vary from a minimum to a maximum value. As mentioned before these two limits are set by adjusting two 10K potentiometers of Fig. C9. From the waveforms of Fig. C12 it is clear that the higher the VCO output signal frequency the wider the pulses at T14. In addition, the frequency of VCO output pulses determines the mode of chopper operation. The final signals (Q), (R), (T) and (U) shown in Fig. C12 depict a motoring chopper operation in which both chopper output current and voltage, Fig. C3, are positive. The high frequency (HF) signals arrived at dual AND gate K result in the thyristor gating signals to be consisted of a train of narrow pulses not shown in Fig. C12 thus preventing the saturation of pulse transformers driving the thyristor gates. The generation of gating signals are inhibited by signals arrived at terminals 36 and 35 in Fig. C11.

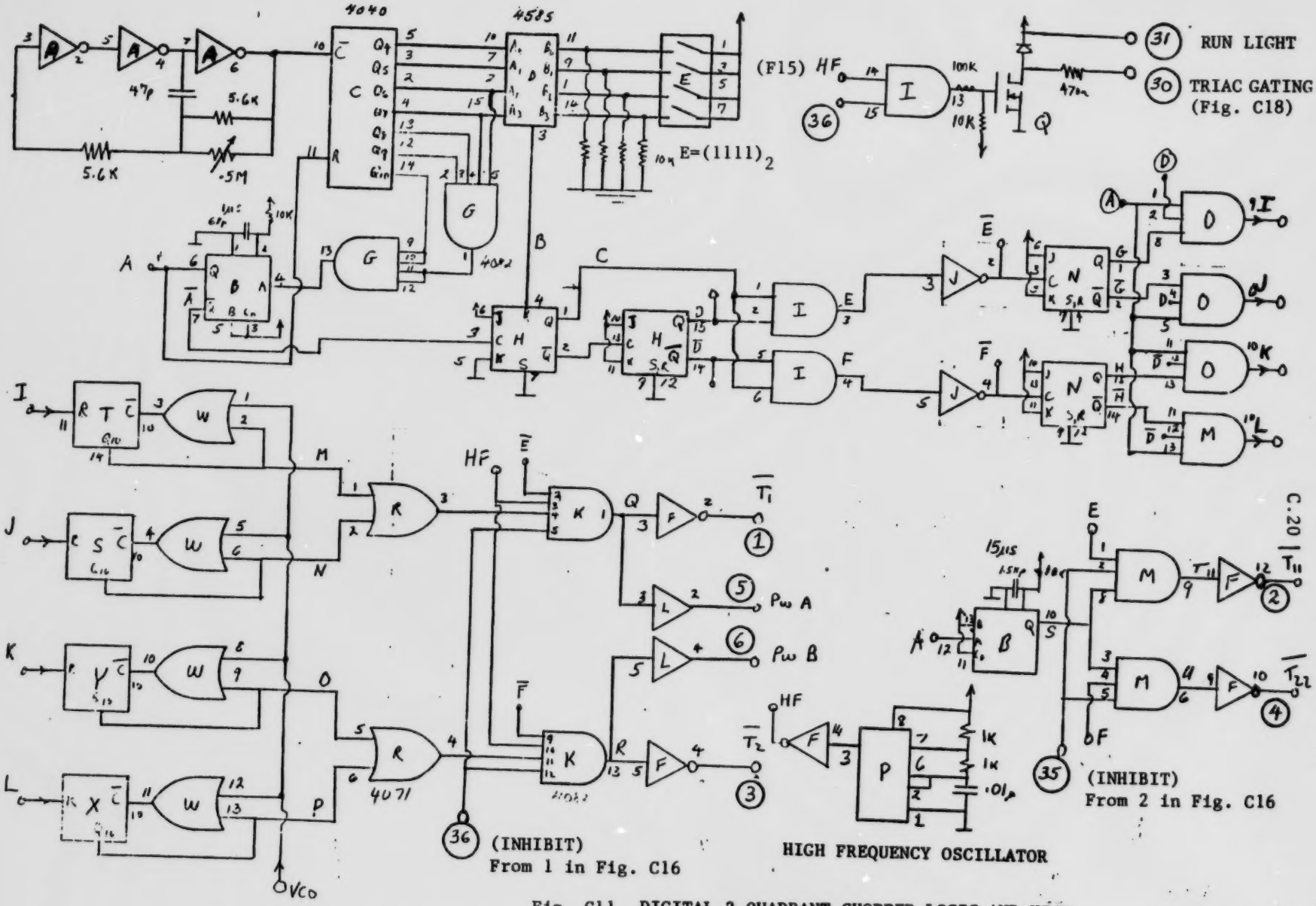


Fig. C11 DIGITAL 2 QUADRANT CHOPPER LOGIC AND HIGH FREQUENCY OSCILLATOR (BOARD A)

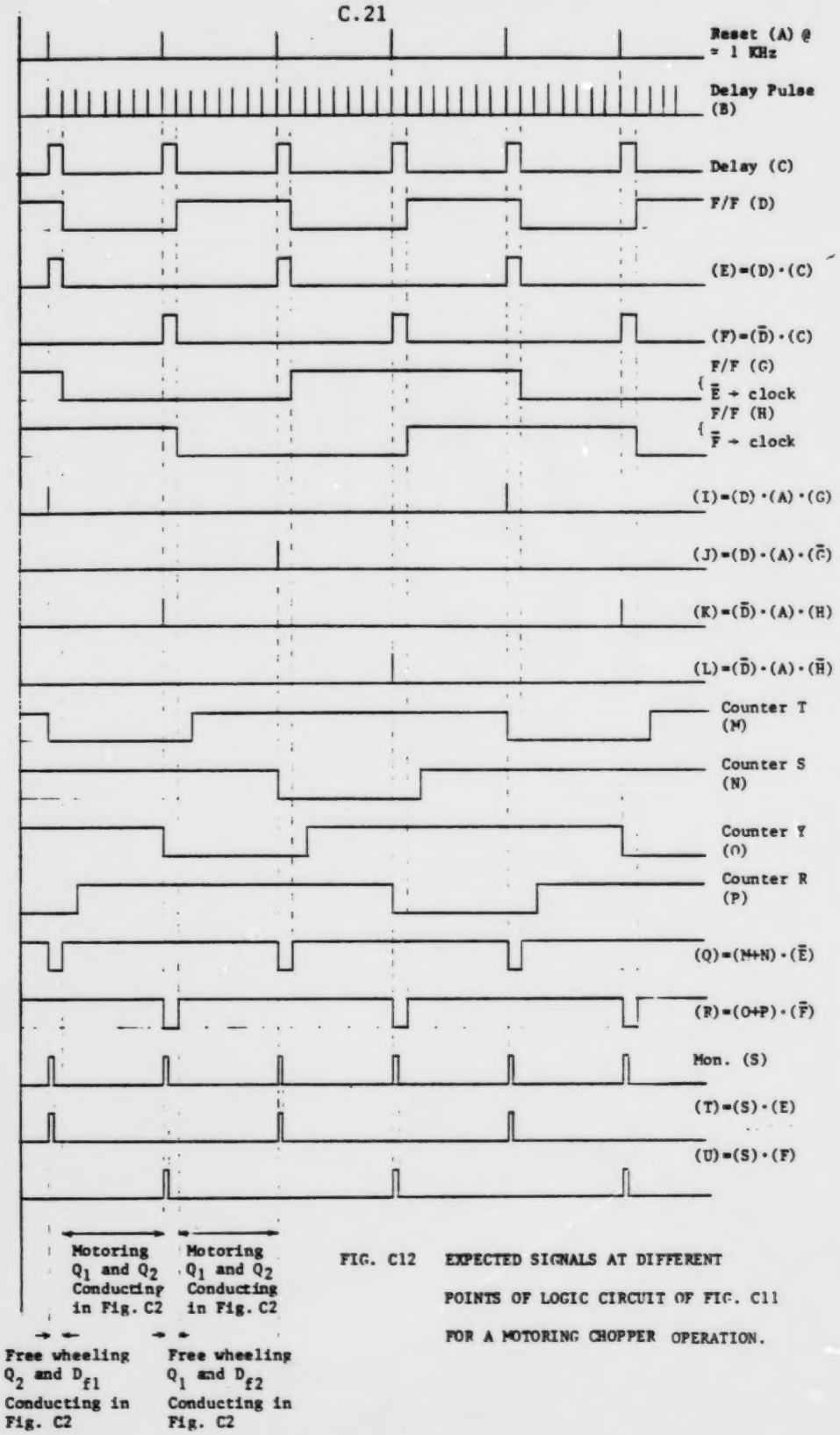


FIG. C12 EXPECTED SIGNALS AT DIFFERENT POINTS OF LOGIC CIRCUIT OF FIG. C11 FOR A MOTORING CHOPPER OPERATION.

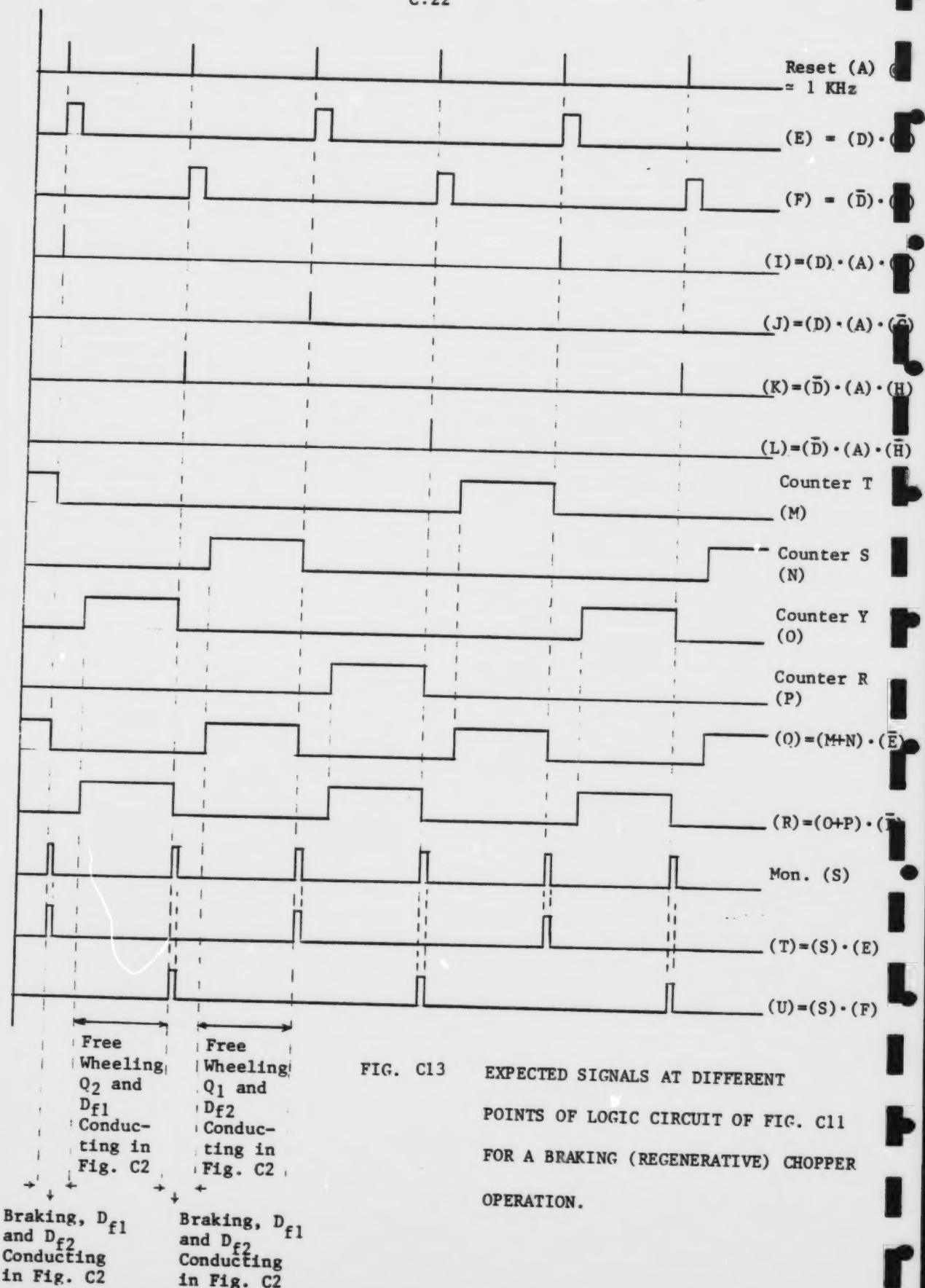


FIG. C13 EXPECTED SIGNALS AT DIFFERENT POINTS OF LOGIC CIRCUIT OF FIG. C11 FOR A BRAKING (REGENERATIVE) CHOPPER OPERATION.

The way these signals are generated are explained later, Fig. C16. Signals (Q), (R), (T) and (U) after being inverted become the inputs to pulse amplifiers, Fig. C17. Signals (PWA) and (PWB) are the same as signals (Q) and (R) and can be connected to an oscilloscope for measuring the actual widths of the main thyristor gatings and to a counter for finding their frequency. From gating signal waveforms the chopper mode of operation (motoring, braking) can also be determined. Figs. C13 shows the waveforms of those signals affected by the frequency of VCO output signals. These waveforms demonstrate the chopper operation in a braking mode.

C3.2.4 Commutation Over Current Detector

To protect the chopper circuit of Fig. C3 against any excessive commutation current which may result in a high voltage across any one of the commutating capacitors the circuit shown in Fig. C14 is employed. This circuit consists of two similar parts. Each part is used for one of the commutating circuits. Considering the upper commutating circuit of Fig. C3, this protective circuit operates as follows. The secondary of current transformer CT.1 is connected across a 1Ω resistor. The voltage produced across this resistor is proportional to commutating current. This voltage is the input signal to difference amplifier U_t. The connection of this voltage to U_t should be done in such a way that by gating Q_{11} in Fig. C3 the voltage at terminal 33, during the first half-cycle of the commutation current, stands higher than that of terminal 34. In this event, the signal appearing at U_t6 has a negative value. This negative voltage after passing through low pass filter V_t yields a positive signal at V_t6. As long as this voltage is smaller than the reference voltage at W_t2, the output of comparator W_t, i.e., K_{11}, stays high. In case of an excessive first half-cycle commutating current the voltage at K_{11} goes "Low" which shuts off the chopper logic circuit, Figs. C16 and C11. The explanation given above also holds for K_9 in Fig. C14.

C3.2.5 Over/Under Voltage Signals

For a proper operation of the chopper circuit of Fig. C3 its input voltage should stay between two specific limits. To protect the operations of the chopper against unacceptable fluctuations of input voltage the logic circuit of Fig. C15 is employed. During normal operation the output of the upper comparator in Fig. C15 remains "High" which results in a "Low" level at terminal C4. This terminal is connected to terminal 10 in Fig. C16. At the same time the output of lower comparator in Fig. C15 is also "High" which makes C2 low. This terminal is connected to terminal 9 in Fig. C16. Should the chopper input voltage exceed a predetermined value the output of upper comparator in Fig. C15 becomes "Low" which results in a "High" C4 which shuts off the thyristor gatings through fig. C16. And if the chopper input voltage decreases below a certain value C2 in Fig. C15 becomes "High" which again prevents the generation of thyristor gatings through Fig. C16.

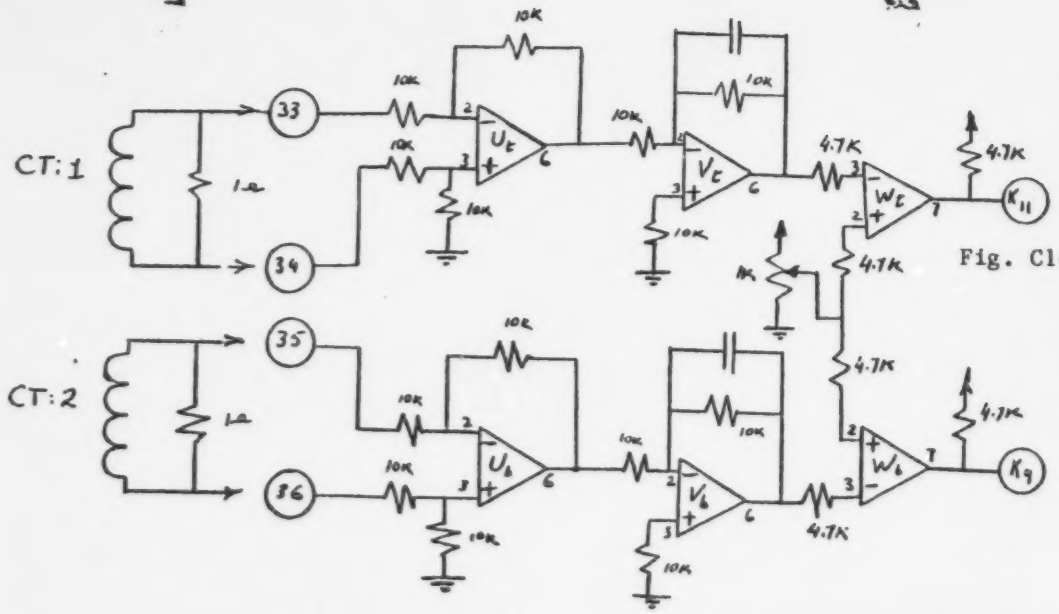


Fig. C14 COMMUTATION OVER CURRENT DETECTION (BOARD B)

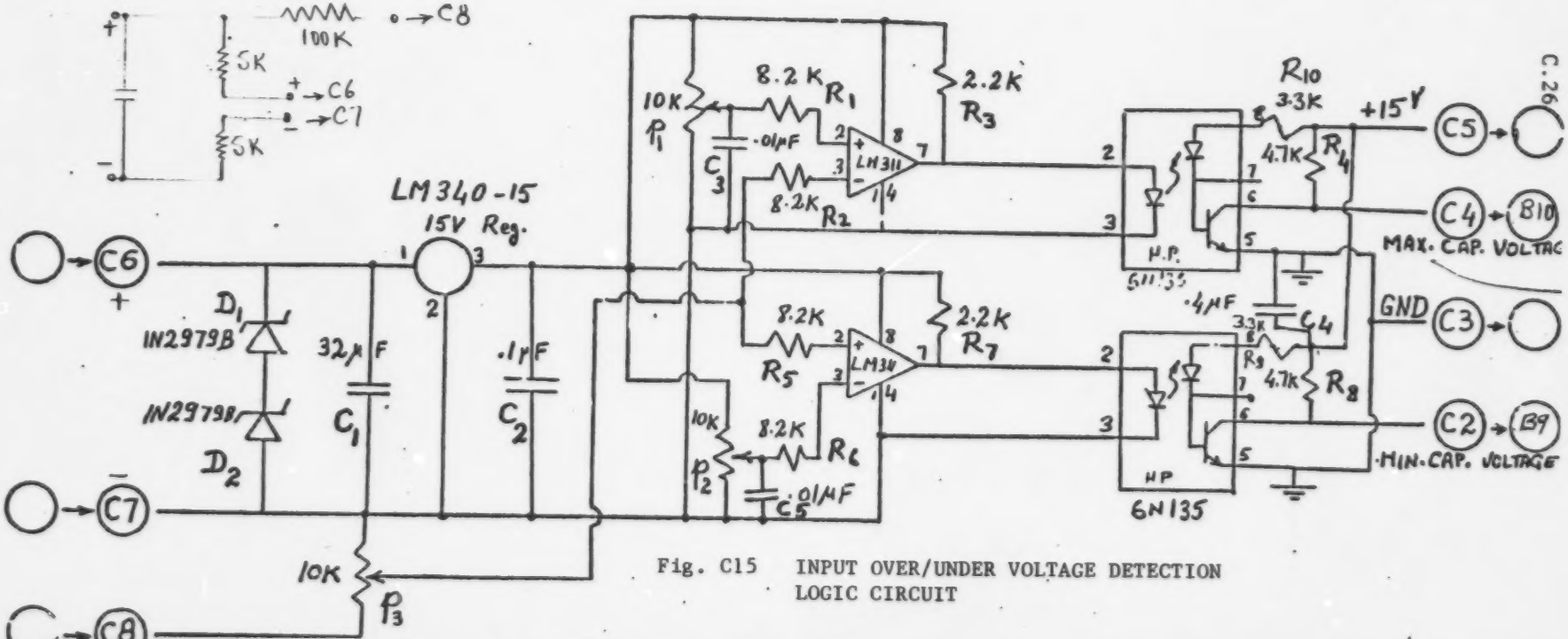


Fig. C15 INPUT OVER/UNDER VOLTAGE DETECTION LOGIC CIRCUIT

C3.2.6 Sequential Start/Stop Logic and Fault Protection Decoding

Fig. C16 shows the logic circuit performing the above functions. To start the generation of gating signals by Fig. C11, "Start" push button in Fig. C16 is first depressed which resets flip-flops G, H and I corresponding to fault signals and assuming the switches connected to G15, H1, H15, I1 and I15 to be all closed the NOR gate Q produces a "High" output at Q13. Upon releasing "Start" push button a positive-going edge of a pulse appears at G3 which sets JK flip-flop G and makes G1 "High". At this moment the two inputs to NAND gate F are both "High" which result in a "Low" output at F10. The outputs of the 4-bit universal shift register B in Fig. C16 immediately after connection of the logic power and before pushing "Start" push button are all "Low". After releasing "Start" push button the "Low" F10 yields a "Low" and a "High" level respectively at B10 and B9 thus putting register B in a shift right mode. By arriving the first clock pulse at B11, B15 (TC) becomes "High" while B12 (TM) remains "Low" which result in a "High" and a "Low" signal at terminals 2 and 1, respectively. These two terminals correspond to terminals 35 and 36 in Fig. C11 so that the commutation thyristors Q_{11} and Q_{22} in Fig. C3 are first gated thus ensuring the proper chopper operation. By arriving the fourth clock pulse at B11, B12 (TM) also becomes "High" and since M2 = Q13 is "High", terminal 1 becomes "High" thus permitting the appearance of main thyristor gating signals at K_1 and K_{13} in Fig. C11.

In case of any malfunction, i.e., upper/lower commutation over current, chopper input over/under voltage, chopper output

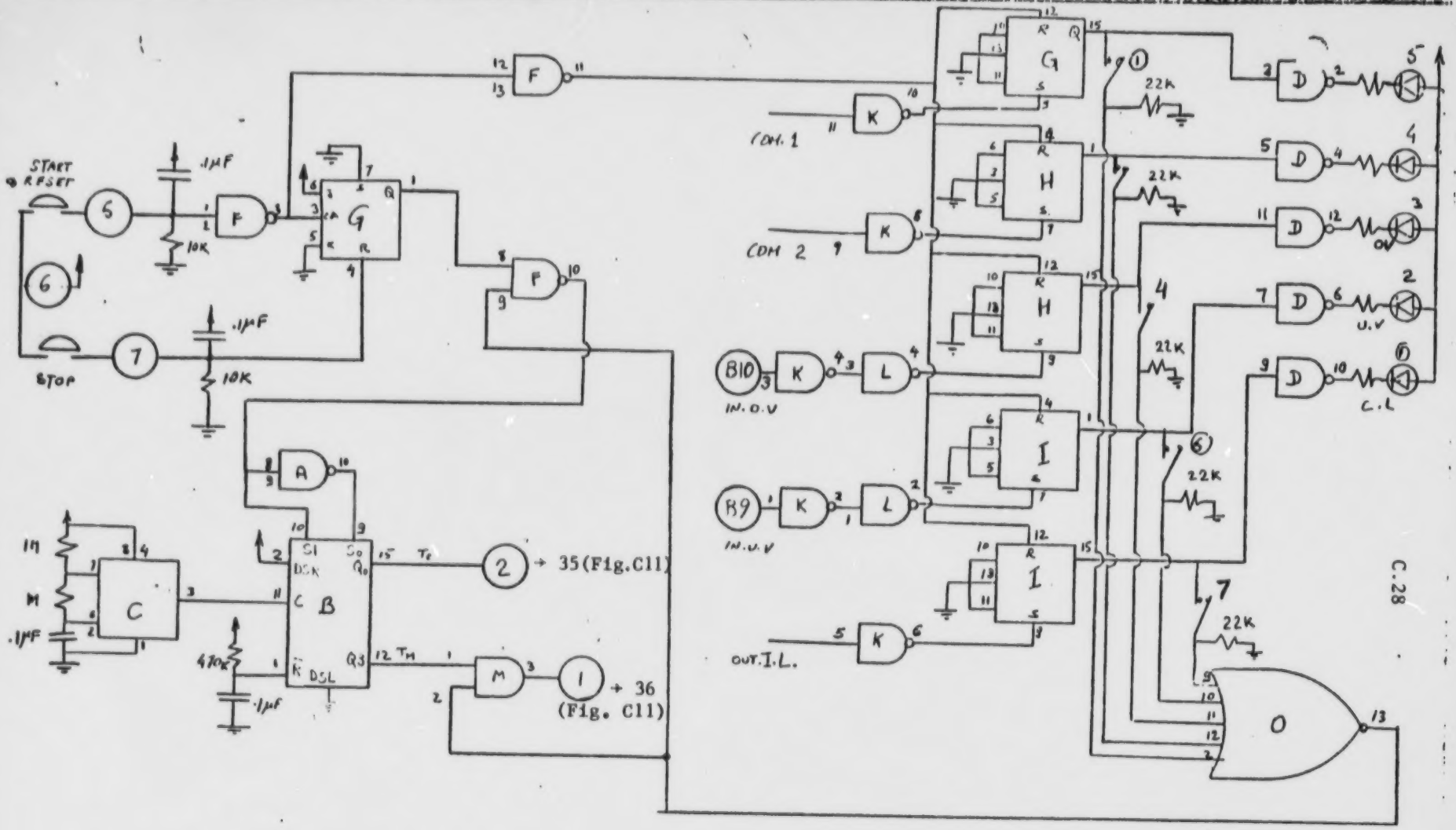


Fig. C16 START/STOP LOGIC AND FAULT PROTECTION DECODING (BOARD B)

instantaneous over current, or by pushing "Stop" push button F10 in Fig. C16 becomes "High" yielding a "High" B10 and a "Low" B9. In this case, B12 (TM) first goes "Low" thus inhibiting the generation of gating signals for the main thyristors in Fig. C11. And since register B now operates in a shift left mode B15 (TC) also becomes "Low" after arriving four clock pulses at B11.

C3.2.7 Pulse Amplifier

The gating signals $\bar{T}_1$, $\bar{T}_2$, $\bar{T}_{11}$ and $\bar{T}_{22}$ generated by the chopper logic circuit of Fig. C11 are the inputs to four similar pulse amplifiers. Fig. C17 shows the layout and the circuit of one of these pulse amplifiers. The output of each pulse amplifier drives a pulse transformer which its secondary output is applied to a thyristor gate. When the input to the pulse amplifier circuit of Fig. C17 is "High" transistor T_1 is on and transistors T_2 and T_3 off so that no output appears at the secondary of the pulse transformer connected to the output. If the input to transistor T_1 goes "Low" this transistor would not conduct and the base of transistor T_2 goes "High" which turns on both T_2 and T_3. In this case a gating pulse is generated across the secondary of a pulse transformer. Note that the gating pulses are the complement of input signals to pulse amplifiers.

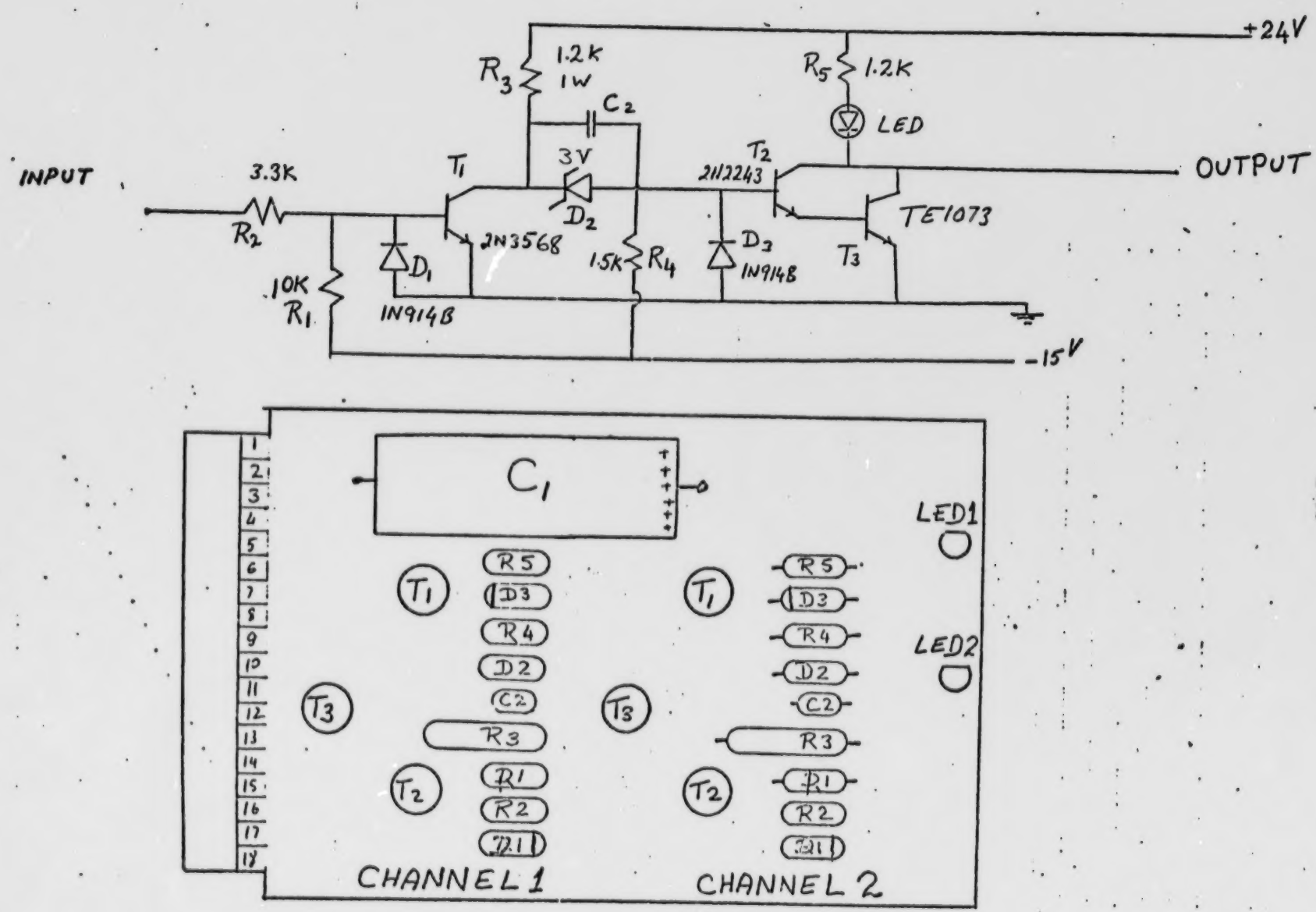


Fig. C17 PULSE AMPLIFIER SCHEMATIC AND BOARD LAYOUT

C3.2.8 Logic Connections

The details of the logic connections are given in Tables C2-C3 and Figs. C18-C24. Table C2 gives the designations of and the interconnections between Boards A and B. Table C3 shows the interconnections between terminal connector L and the other connectors in the logic circuit. Fig. C18 demonstrates the circuit employed in turning on the Run Light when the logic circuit of Fig. C11 operates normally. Fig. C19 gives the logic power supply terminals while Fig. C20 shows the connections of the chopper input under and over voltage protection card. Figs. C21 and C22 display the pulse amplifier and protection terminals for the lower and upper semiconductor groups of Fig. C2. Finally, Figs. C23 and C24 show the chopper front panel view and the corresponding wiring.

A1	T_1 Gating	B1	T_M (INHIBIT)
2	T_{11} "	2	T_L (INHIBIT)
3	T_2 "	3	
4	T_{22} "	4	
5	P.W. Upper Chopper	5	Start P.B.
6	P.W. Lower Chopper	6	+15 V_{OUT}
7		7	Stop P.B
8		8	GND
9		9	Under Voltage
10	P.W. Control - Open-Loop	10	Over Voltage
11	P.W Control - Closed-Loop	11	+15 V out
12	−15 V_{IN} S_6	12	−15 V_{IN} S_6
13		13	
14		14	
15	GND S_5	15	GND S_5
16		16	
17		17	
18		18	
19		19	
20		20	
21		21	
22		22	
23		23	
24	+15 V_{IN} S_4	24	+15 V_{IN} S_4
25		25	
26		26	
27		27	P.W. Output
28		28	} P.I. - R.C Lo
29		29	
30		30	Demand To P.W. Controller
31		31	} + Hall Current Feedback
32		32	} − Signal
33		33	} - C.T. Current Feedback
34		34	} - Signal Upper Chopper
35	T_L (INHIBIT)	35	} - C.T. Current Feedback
36	T_M (INHIBIT)	36	} - Signal Lower Chopper

(a) AUGAT BOARD DESIGNATIONS

A10	B30	A34	B3
A11	B27	A35	B2
A33	B4	A36	B1

(b) AUGAT BOARD INTERCONNECTION

TABLE C2 BOARDS A AND B DESIGNATIONS AND INTERCONNECTIONS

	Q_5		L1	A_1	T_1
	Q_7		2	A_2	T_{11}
	Q_6, O_6		3	GND	
	O_5		4	A_3	T_2
	O_7		5	A_4	T_{22}
TO FREQ COUNTER'S	M_1		6	A_5	
	M_3		7	GND	
	M_2		8	A_6	
			9		
TO FRONT POT	M_4	(+15V)	10	L_{14}	
	M_5	(WIPER)	11		
	M_6	(GND)	12	A_{19}	
			13	A_{10}, B_{30}	
		(+15V)	14	A_{20}	
			15		
			16		
			17		
RUN LIGHT TRIAC.	T_2	(VMOS-D)	18	A_{30}	
	T_1	(+15V)	19	A_{31}	
START	M_9		20	B_5	
GND	M_7		21	B_6	
STOP	M_8		22	B_7	
+15	M_{17}		23	B_8	
UNDER. V.	M_{18}		24	B_9	
OVER. V.	M_{19}		25	B_{10}	
GND	M_{20}		26	B_{11}	
P.I. OUTPUT			27	B_{27}	
P.I.-R.C.			28	B_{28}	
			29	B_{29}	
			30		
FRONT POT.	M_5 (WIPER)		31	B_{30}, A_{10}	
HALL SHIELD			32	GND	
HALL	E_6		33	B_{31}	
	E_5		34	B_{32}	
			35		
COMM. #1 C.T.	P_{11}		36	B_{33}	
	P_{12}		37	N.C.	
	P_{13}		38	B_{34}	
COMM #2 C.T.	N_{11}		39	B_{35}	
	N_{12}		40	N.C.	
	N_{13}		41	B_{36}	
			42		
STAND-BY LIGHT	M_{10}		43	L_{48}	
	M_{11}	RUN LIGHT	44	L_{47}	
	M_{12}		45	T_4	
			46		
110 V_{AC} IN	S_1		47	To L_{44}	
	S_2		48	To L_{43}, T_3	

TABLE C3 "L" CONNECTOR TERMINAL STRIP

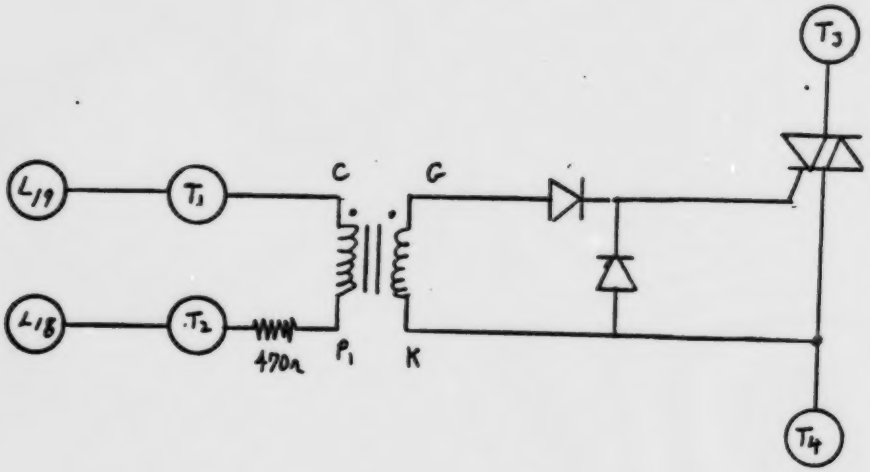


FIG. C18 RUN LIGHT TRIAC GATING

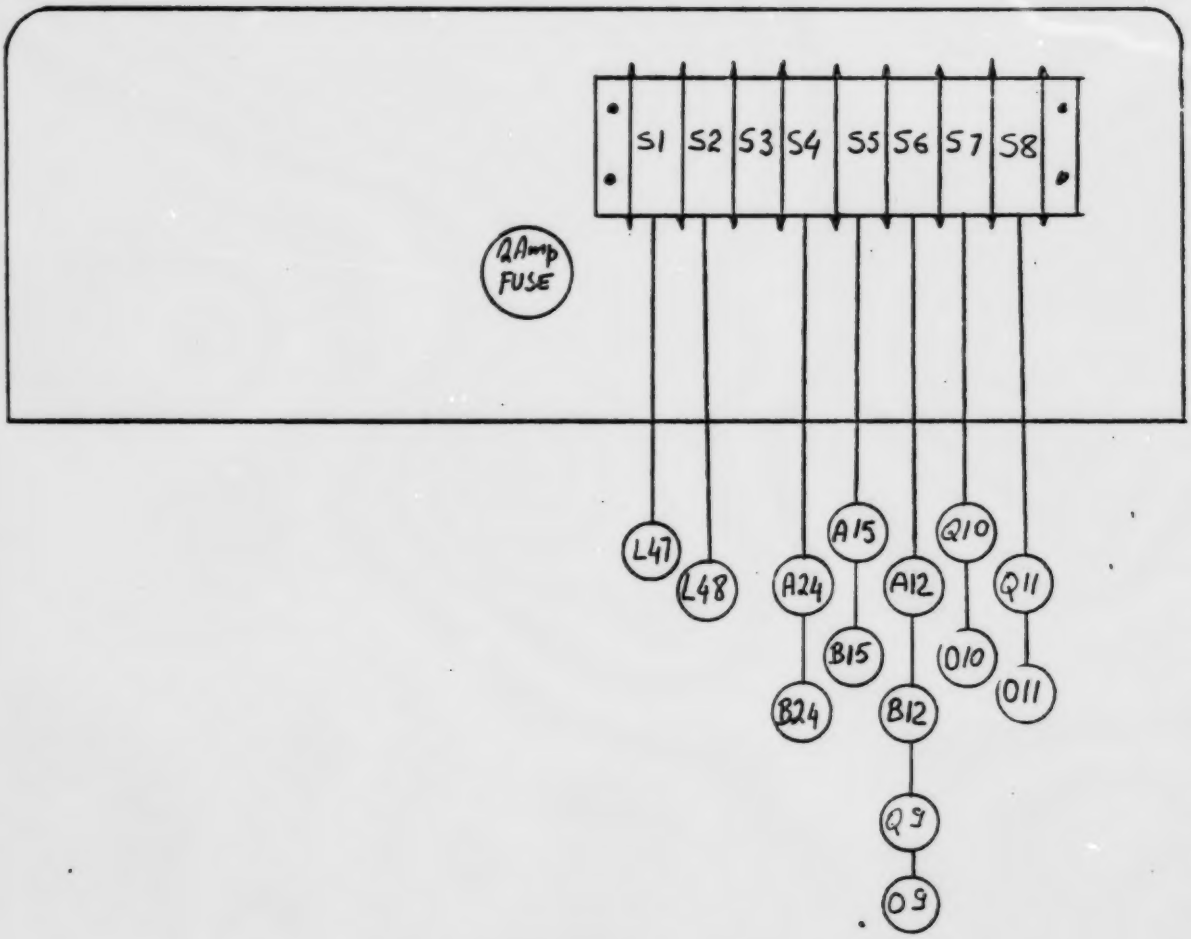


FIG. C19 POWER SUPPLY TERMINALS

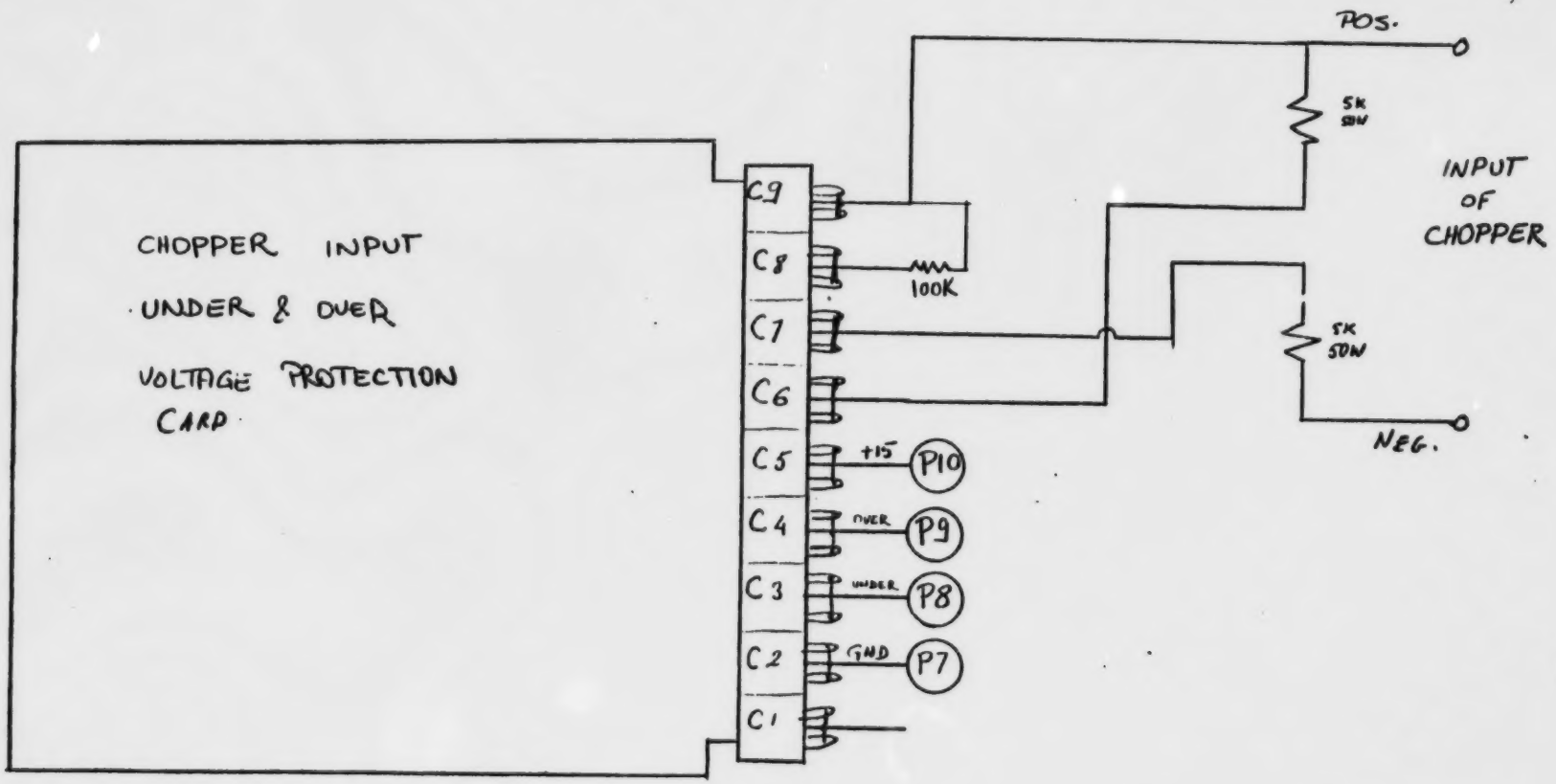


FIG. C20 UNDER AND OVER VOLTAGE CARD CONNECTIONS

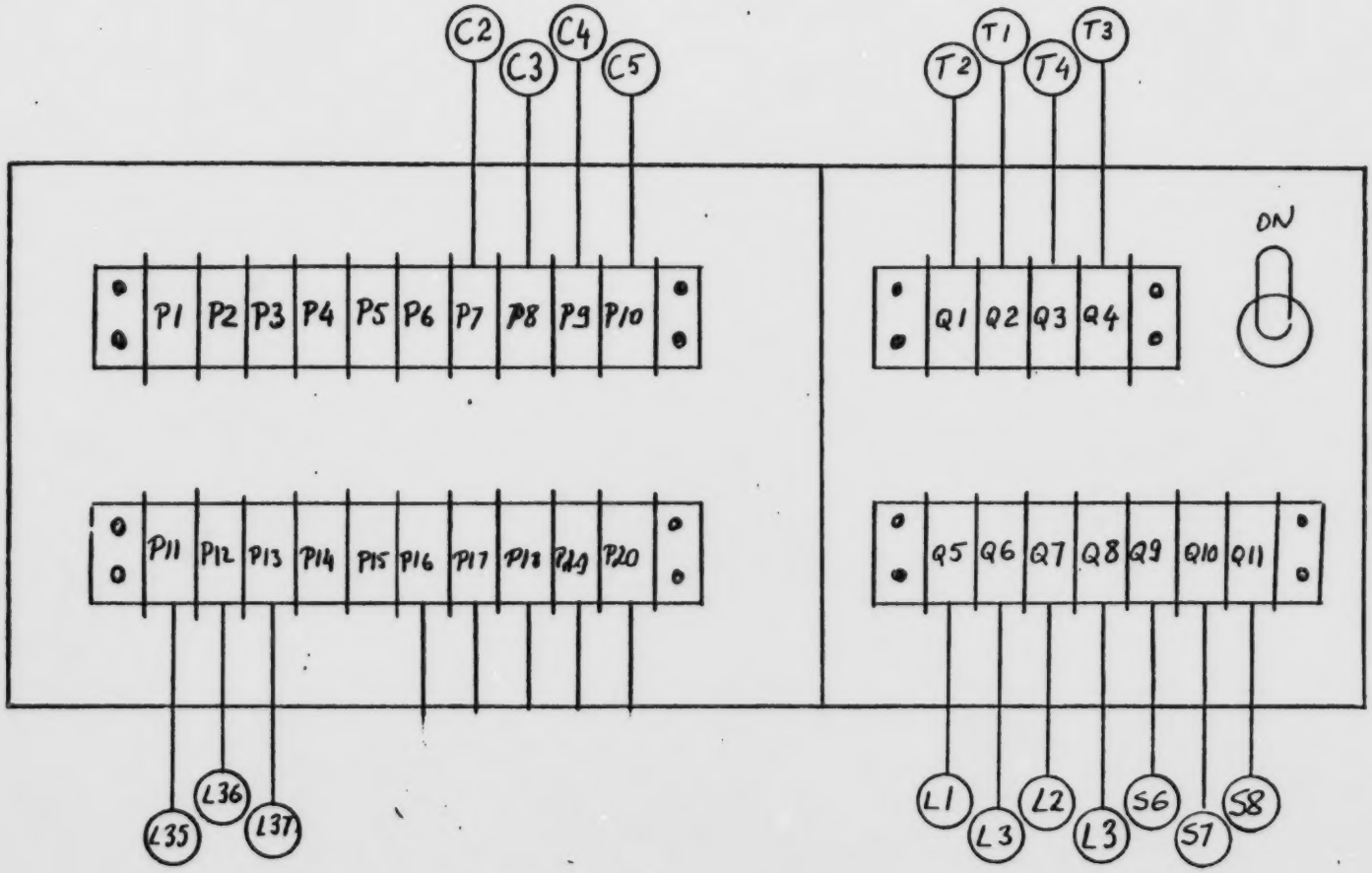


FIG. C21 TOP SHELF PULSE AMPLIFIER AND PROTECTION TERMINALS

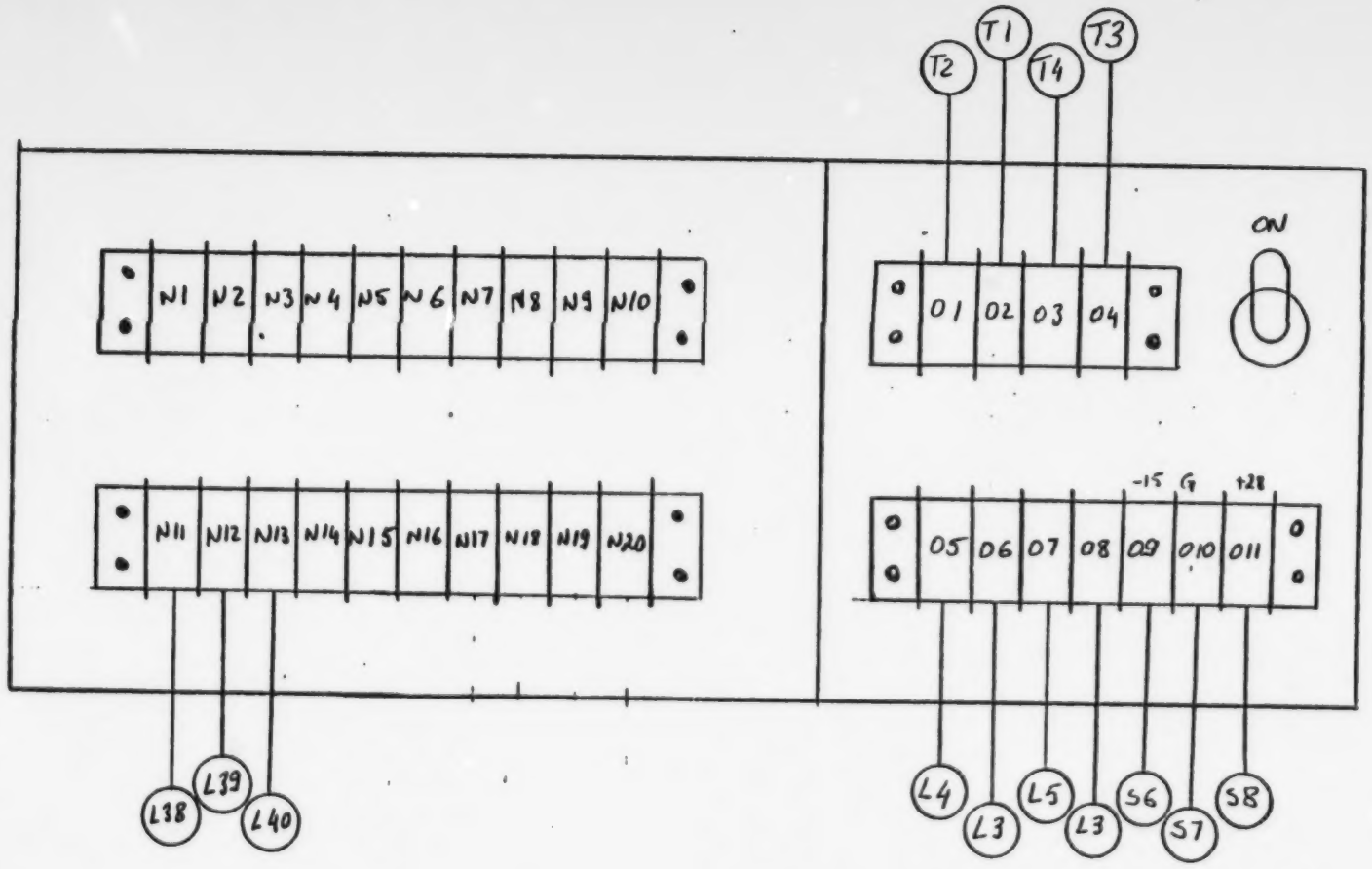


FIG. C22 BOTTOM SHELF PULSE AMPLIFIER AND PROTECTION TERMINATIONS

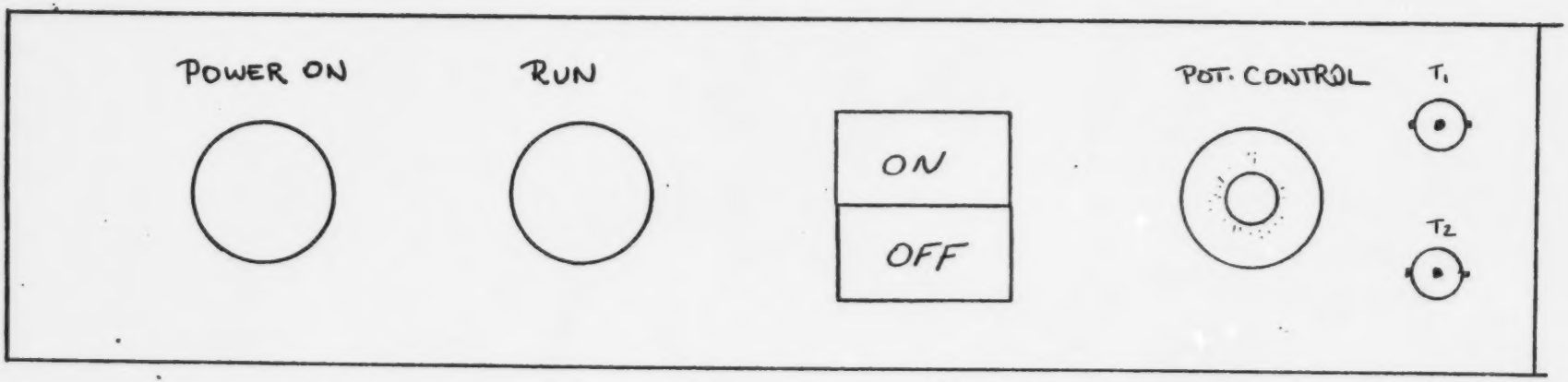


FIG. C23 2 QUADRANT CHOPPER - FRONT PANEL

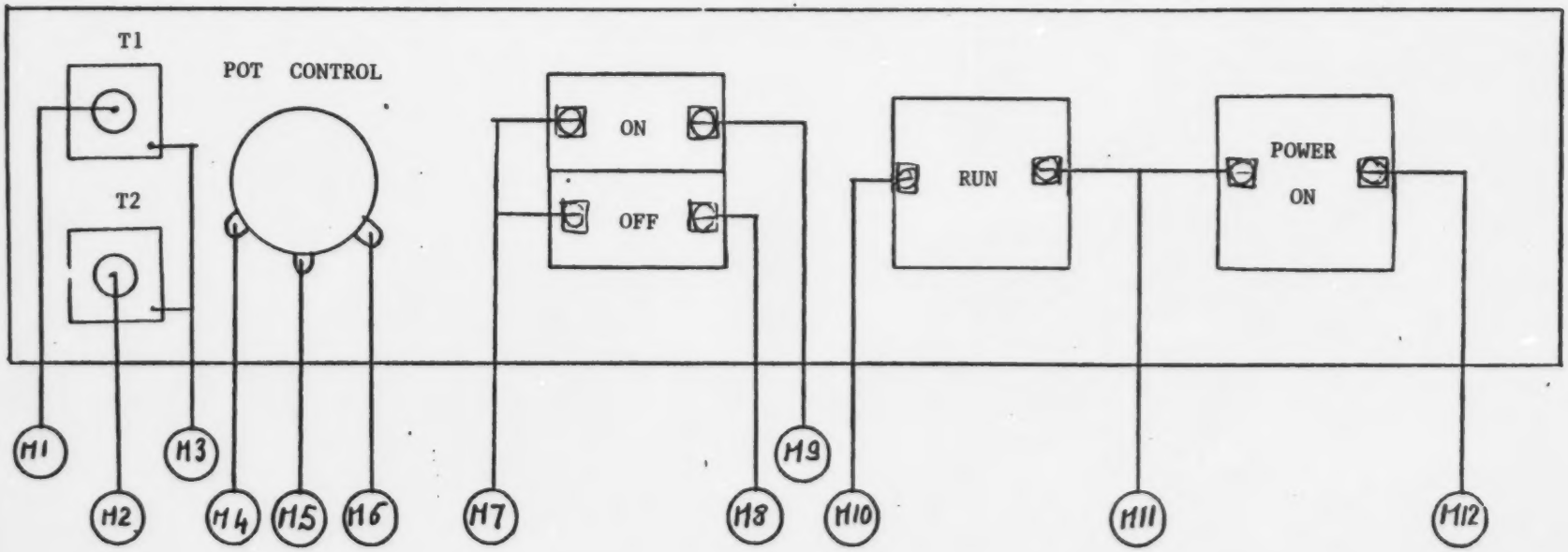


FIG. C24 2 QUADRANT CHOPPER - FRONT PANEL WIRING

APPENDIX D

CURRENT SOURCE INVERTER UNIT

APPENDIX D

CURRENT SOURCE INVERTER UNIT

D1 Introduction

There are two current-source inverters in the test set-up. These inverters are quite similar to each other so that the specifications and the detailed description given in the following applies only to one unit. Each inverter is supplied by the chopper current source with a unidirectional current and a bidirectional voltage. The loading of each ac motor, driven by the corresponding current source inverter, is performed by loading a separately excited dc machine mounted on its shaft.

D2 Specifications

The block diagram of a current source inverter unit is shown in Fig. D1. The inverter can drive a 125-HP ac squirrel cage induction motor, with both 230V and 460V, which corresponds to the series or parallel connections of two inverters, respectively. Only motoring and braking modes of operation are considered here. The inverter frequency range is from 0 to 150 Hz (4,000 rpm maximum motor speed). The inverter design is modular such that the value of the commutation capacitors can be changed easily. Some of the other features of the design are:

(1) All the major components are water cooled such that the system losses can be measured with water flow and temperature measurements.

(2) The logic is designed such that automatic gating of the inverter thyristors occurs if any overvoltage condition occurs. An overvoltage protection in C.S.I. is necessary to avoid open connection or malfunction of the inverter with the resulting damage to the semiconductor components.

(3) The logic is designed such that both the slip frequency and power factor control can be tested by replacing a logic board. The system test results therefore can be obtained both with the slip frequency and the power factor control.

(4) An instrumentation unit is designed which provides two isolated inverter output voltages with isolation amplifiers, two isolated phase current signals with Hall amplifiers, analog signal for the

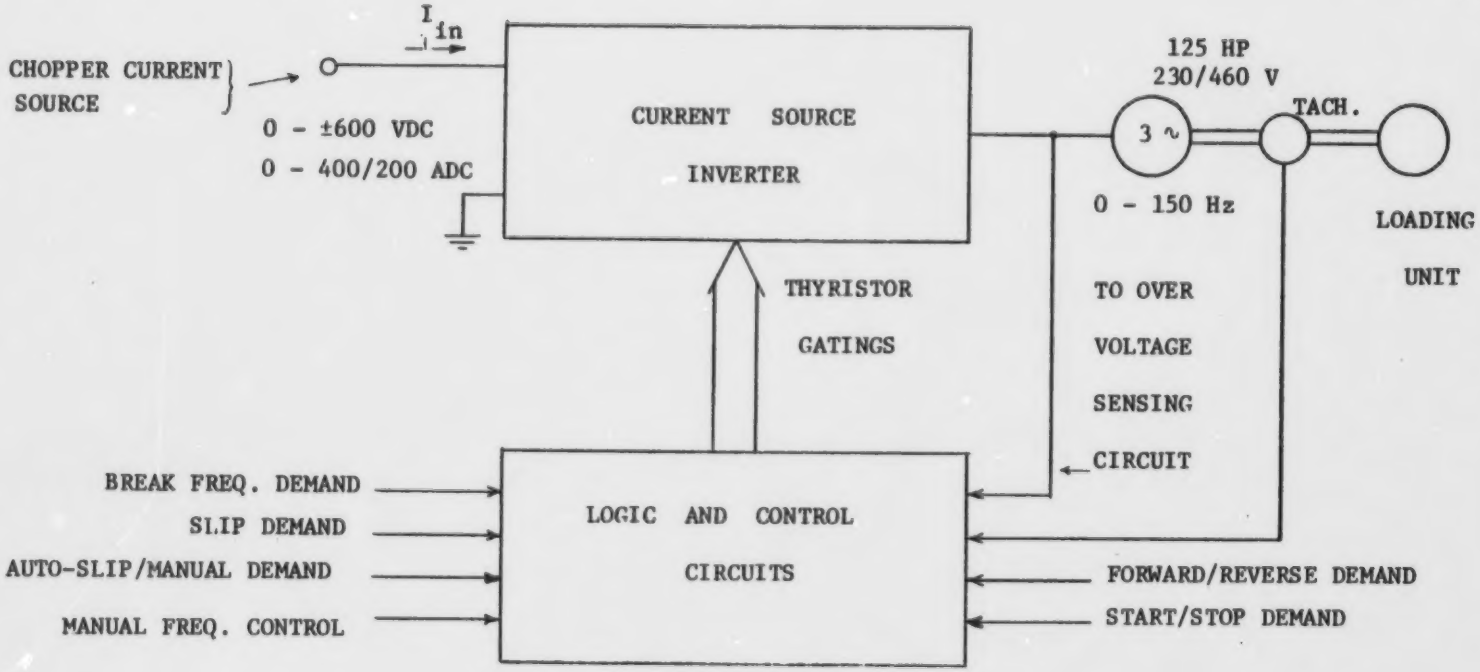


FIG. D1 BLOCK DIAGRAM OF A CURRENT SOURCE INVERTER OPERATION DRIVING ONE 125-HP MOTOR

three phase power, analog signals for rms and fundamental output voltage and current, motor power factor and output frequency.

(5) The inverter can operate in all four quadrants of the speed-torque curve by small signal logic control. The reversal is achieved at zero current by modifying the inverter gating such that the output voltage phase sequence is reversed.

D3 Detailed System Description

In the block diagram of Fig. 1.1 two current source inverters were shown, each of which can drive a 125-HP induction motor with a nominal voltage, either equal to 230 V or 460 V and with an adjustable output frequency from 0 to 150 Hz. The power, logic and control circuits of these two inverters are quite similar to each other so that the explanations given here apply only to one inverter unit. In this section the following sub-sections are described in detail:

(1) Inverter Power Circuit

(2) Logic, Control and Protection Circuits

(3) Determination of Motor Slip

D3.1 Inverter Power Circuit

Fig. D2 shows the simplified power circuit of the current source inverter. The inverter receives its input DC current from the chopper current source (Fig. 1.1) through a smoothing reactor. The polarity of the input voltage to the inverter as shown in Fig. D2 denotes a motoring operation while the voltage reversal indicates a regeneration. Thyristors Q_1 to Q_6 are invertor-type SCR's with small turn-off times which are protected against excessive di/dt by inductances L_1-L_6. Capacitors C_a, C_b, C_c, C_r, C_s and C_t along with the load inductances provide the necessary forced commutation for thyristors. The peak voltage appearing across any two output terminals is the same as the peak voltage of commutating capacitors. Corresponding to each SCR two isolating diodes are connected in series. The reverse voltage across the two isolating diodes in series with each thyristor is almost twice that of the capacitor peak voltage. The resistance R_{sh} in Fig. D2 is a shunt resistance across which a connected ampmeter shows the magnitude of the DC link current. The detailed inverter power circuit is shown in Fig. D3. In this figure R_v and C_v are the snubber, resistance and capacitance protecting thyristors and diodes against excessive dv/dt. Terminal numbers are also shown in Fig. D3. The specifications of the components used in building the circuit of Fig. D3 are shown in Table D1.

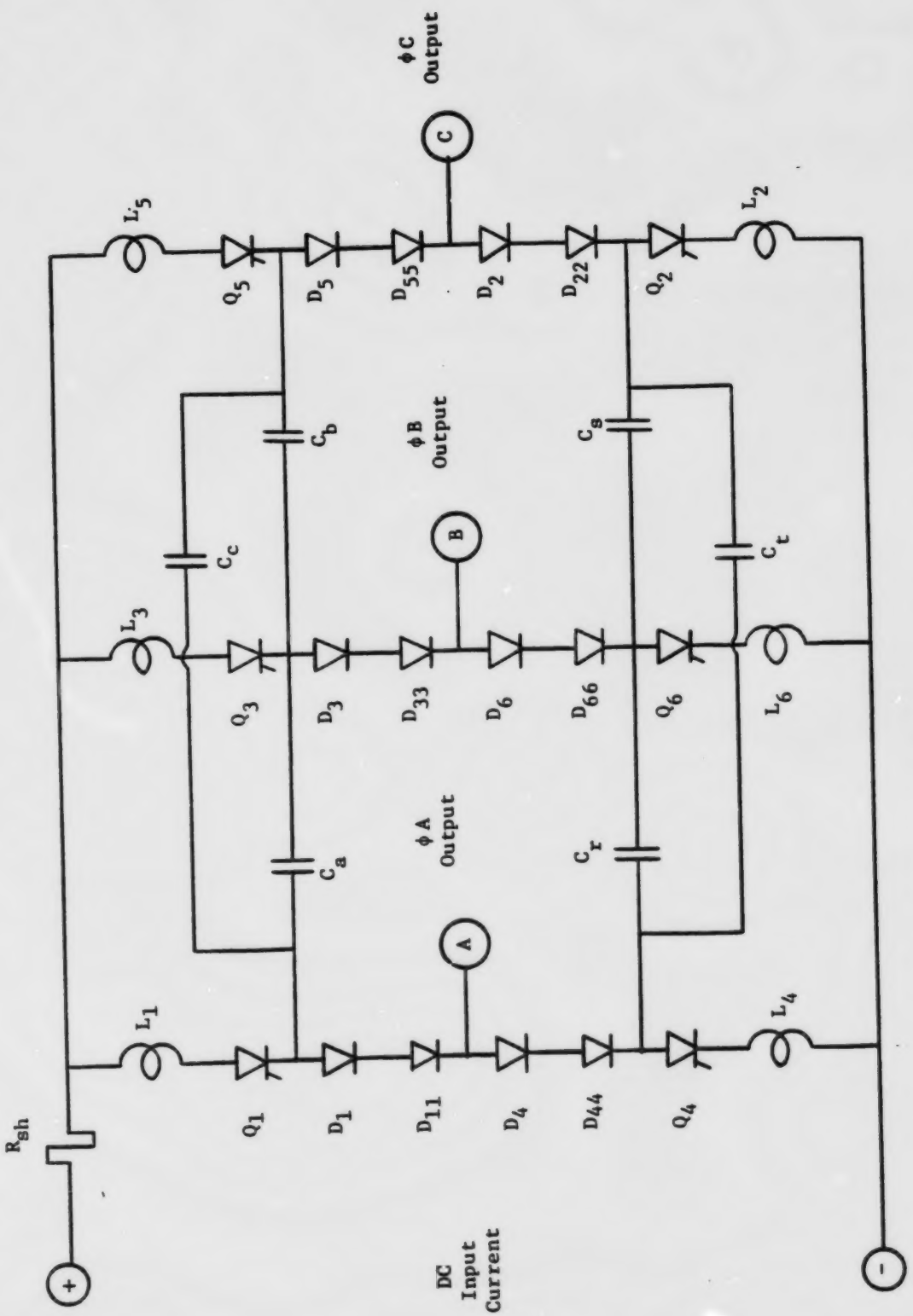


FIG. D2 3-PHASE CURRENT SOURCE INVERTER - POWER CIRCUIT

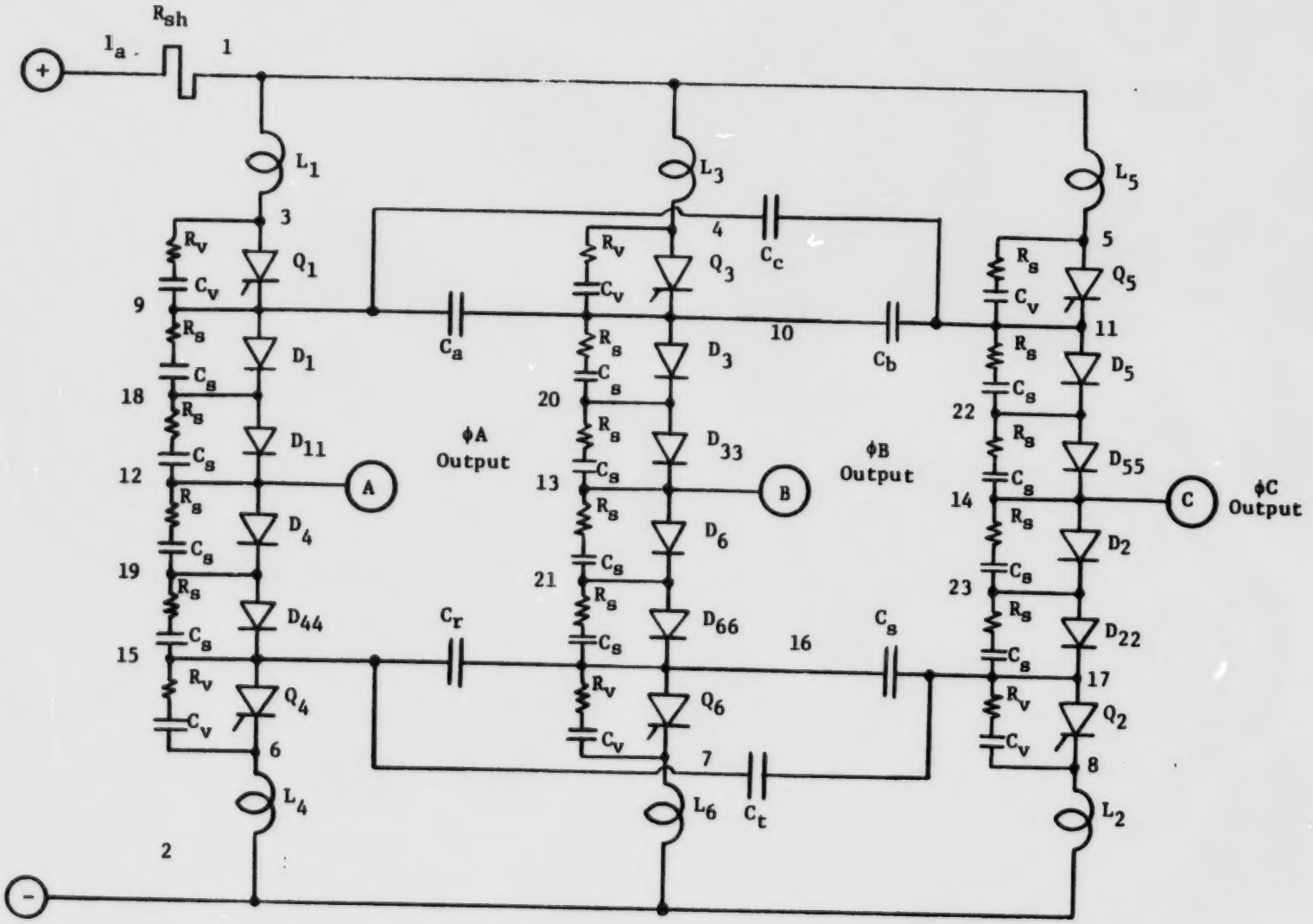


FIG. D3 3-PHASE CURRENT SOURCE INVERTER - DETAILED POWER CIRCUIT

Component	Specifications
Thyristors Q_1-Q_6	Westcode, D1197TH18/CH2H0, 600A, 1800V
Diodes D_1-D_6, D_{11}-D_{66}	Westinghouse, R6222035A, 350A, 2000V
Capacitors C_a,C_b,C_c,C_r, C_s,C_t	GE, 28F5137FC, 20 μF, 1000V 3 in parallel for 60 μF
Inductors L_1-L_6	15 turns 3/8" tubes, taps on 8th, 10th, 13th and 15th turn, 3½" diam., ≈1μH/turn
H.E. current transducer	OSI, CT600LS, 600A
Snubber resistors R_v Snubber capacitors C_v	10Ω, 100 W, Ohmite, non-inductive .5 μF, 2000V peak
Voltmeter, input Ampmeter, input	750 - 0 - 750 VDC 0 - 500 ADC
Shunt R_{sh}	500A, 50 mV

TABLE D1 SPECIFICATIONS OF THE COMPONENTS IN THE INVERTER POWER CIRCUIT OF FIG. D3.

D3.2 Logic and control circuits

The block diagram of the inverter logic system for motor slip control is shown in Fig. D4. The inputs to Fig. D4 after being processed in different parts of the logic system lead to generation of required gating pulses for firing inverter thyristors. In this sub-section the following parts are covered:

(1) Tachometer Signal Conditioning Logic

(2) Slip Recovery Logic

(3) Three-Phase Current Source Logic

(4) Inverter Output Over Voltage Protection

(5) Start/Stop Logic

(6) Pulse Amplifier

(7) Logic Layout and Connections

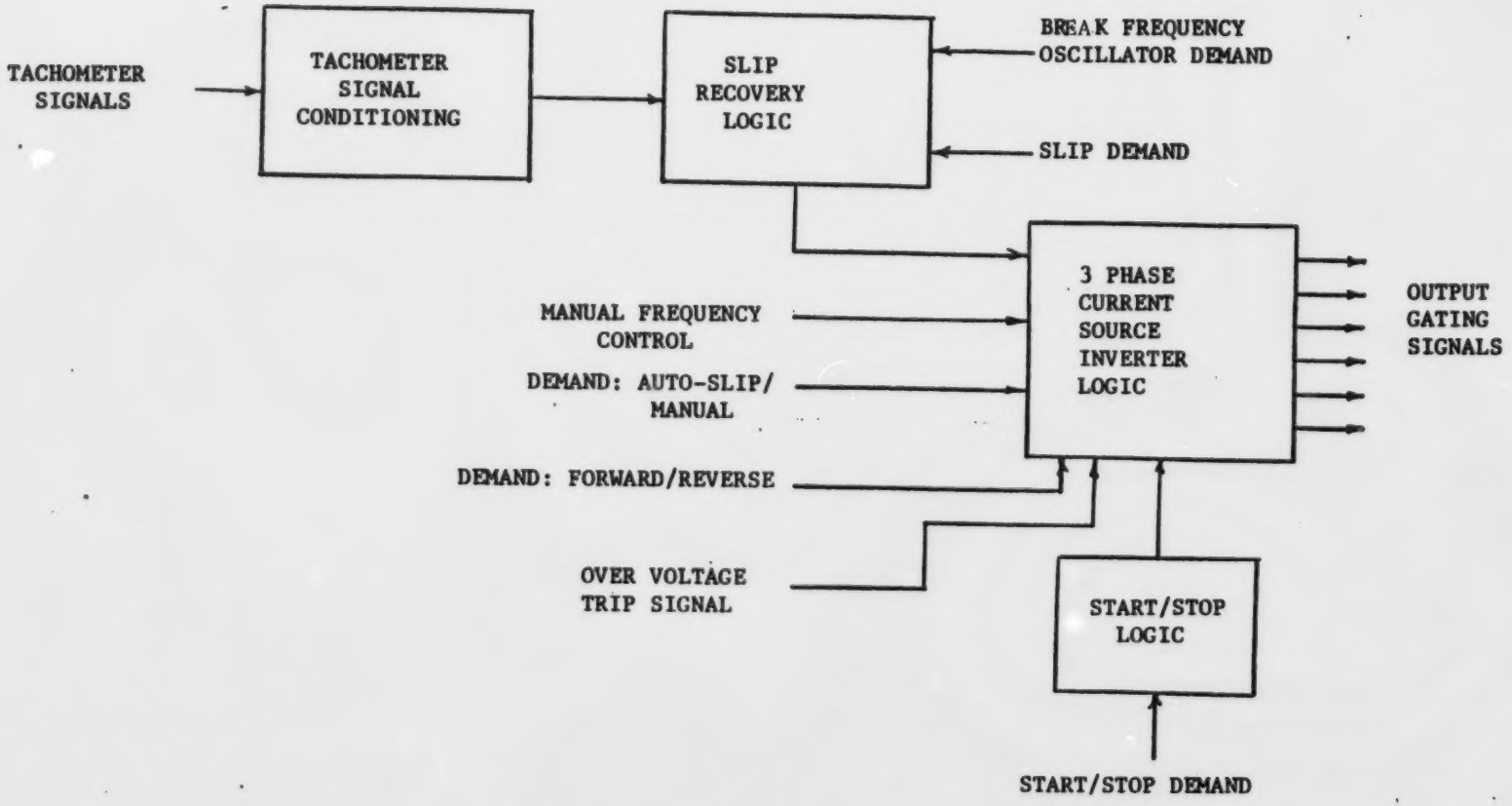


FIG. D4 BLOCK DIAGRAM: SLIP RECOVERY LOGIC SYSTEM

D3.2.1 Tachometer Signal Conditioning Logic

Fig. D5 shows the tachometer signal conditioning logic circuit. The input to this circuit are the signals received from a tachometer mounted on the motor shaft. The tachometer output terminals are connected to terminals A1-A2 in Fig. D5. The frequency of tachometer output signals is directly proportional to the rotor rotational frequency, fm. The proportionality factor, called z, depends on the tachometer construction. Assuming a sinusoidal tachometer output, Fig. D6 shows the expected signal waveforms at different points of the circuit of Fig. D5. The output of this circuit, D1, is one of the inputs to the slip recovery logic explained in the next part.

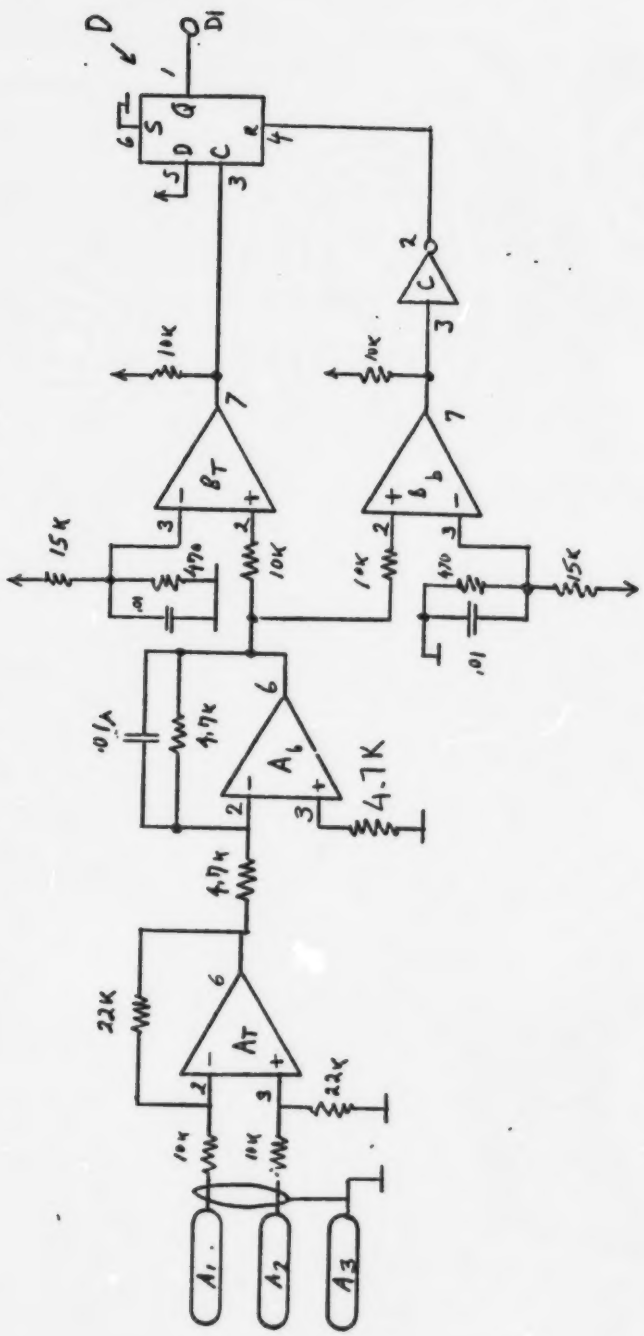


Fig. D5 TACHOMETER SIGNAL CONDITIONING

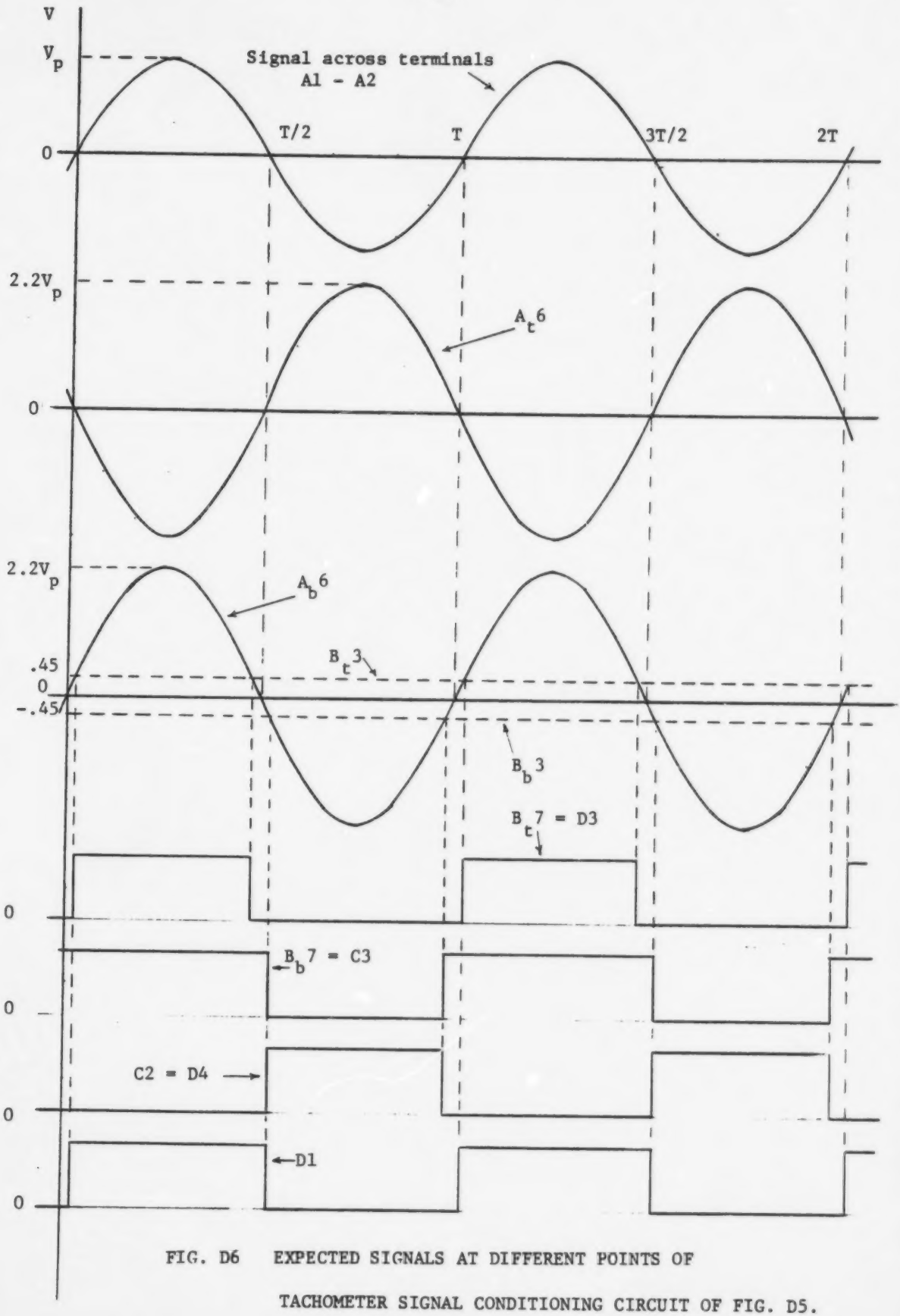


FIG. D6 EXPECTED SIGNALS AT DIFFERENT POINTS OF TACHOMETER SIGNAL CONDITIONING CIRCUIT OF FIG. D5.

D3.2.2 Slip Recovery Logic

The slip recovery logic whose circuit is shown in Fig. D7 provides signals which are fed into the inverter logic circuit as displayed in the block diagram of Fig. D4. The relationship between the frequency of the output signals of Fig. D7 at U10 and that of the input signals to the tachometer signal conditioning logic (Fig. D5) determines the motor slip. The slip recovery logic has been designed so that, in a motoring operation, the motor slip gradually decreases as the motor speeds up. This trend continues until the stator frequency reaches a predetermined value called "break frequency". The slip would then be kept constant irrespective of the stator frequency. In the braking mode of operation the stator frequency, while the slip is kept constant, is decreased up to the break frequency following which the motor slip is gradually increased until the motor is brought to a complete stand. The functions mentioned above are performed by different parts of Fig. D7 as explained in the following and specified in the same figure. Fig. D8 shows the layout and code numbers of IC chips used in the circuits of Figs. D5 and D7.

(1) Break Frequency Oscillator: The break frequency as explained previously is generated by the components specified in Fig. D7. This frequency is adjustable by changing a potentiometer connected to terminal A8 in Fig. D7 and supplied by a negative voltage. The generated ramp waveforms at $K_t 6$ result in a series of narrow pulses at terminal 10 of monostable L. The frequency of these pulses,

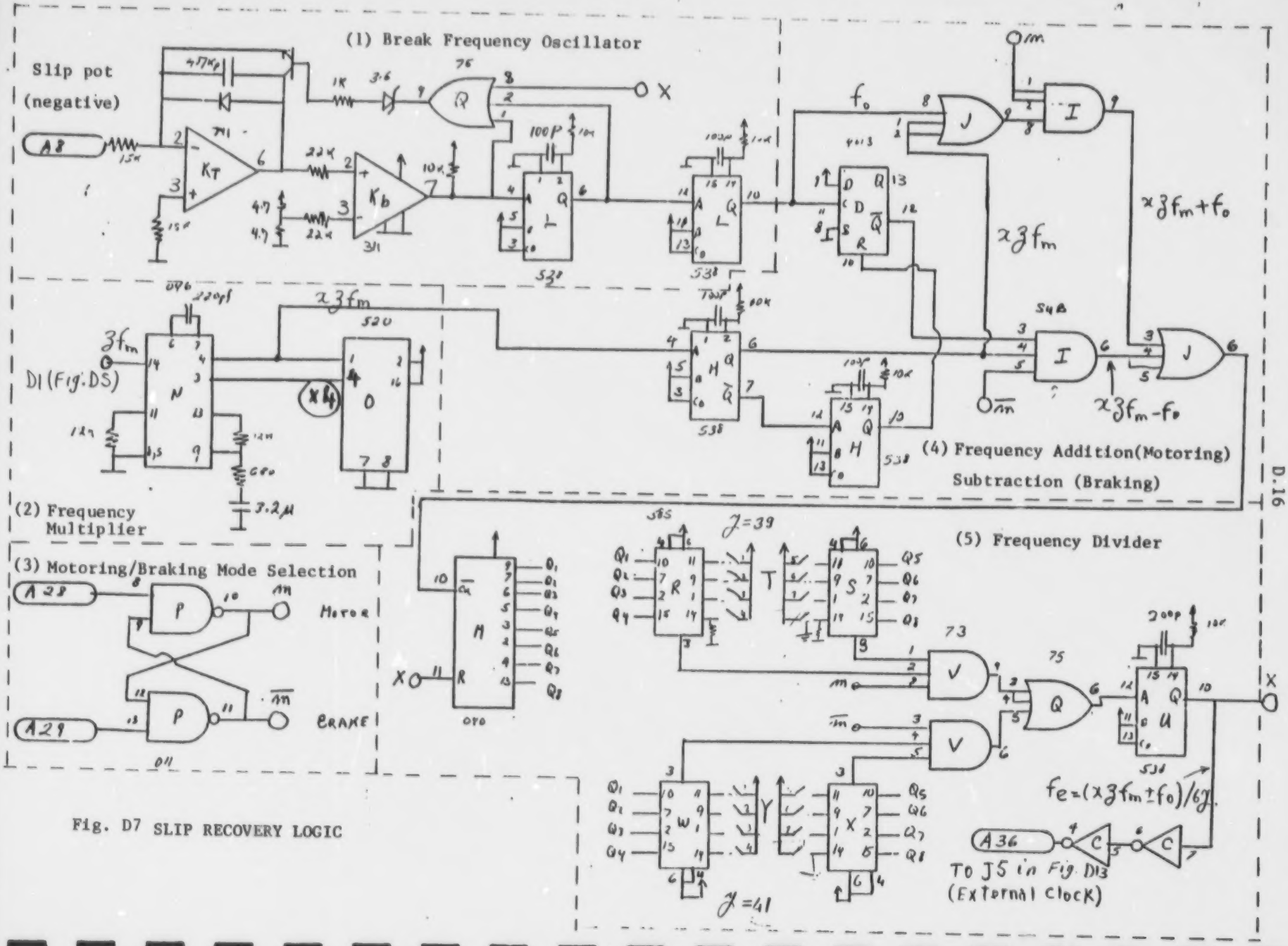


Fig. D7 SLIP RECOVERY LOGIC

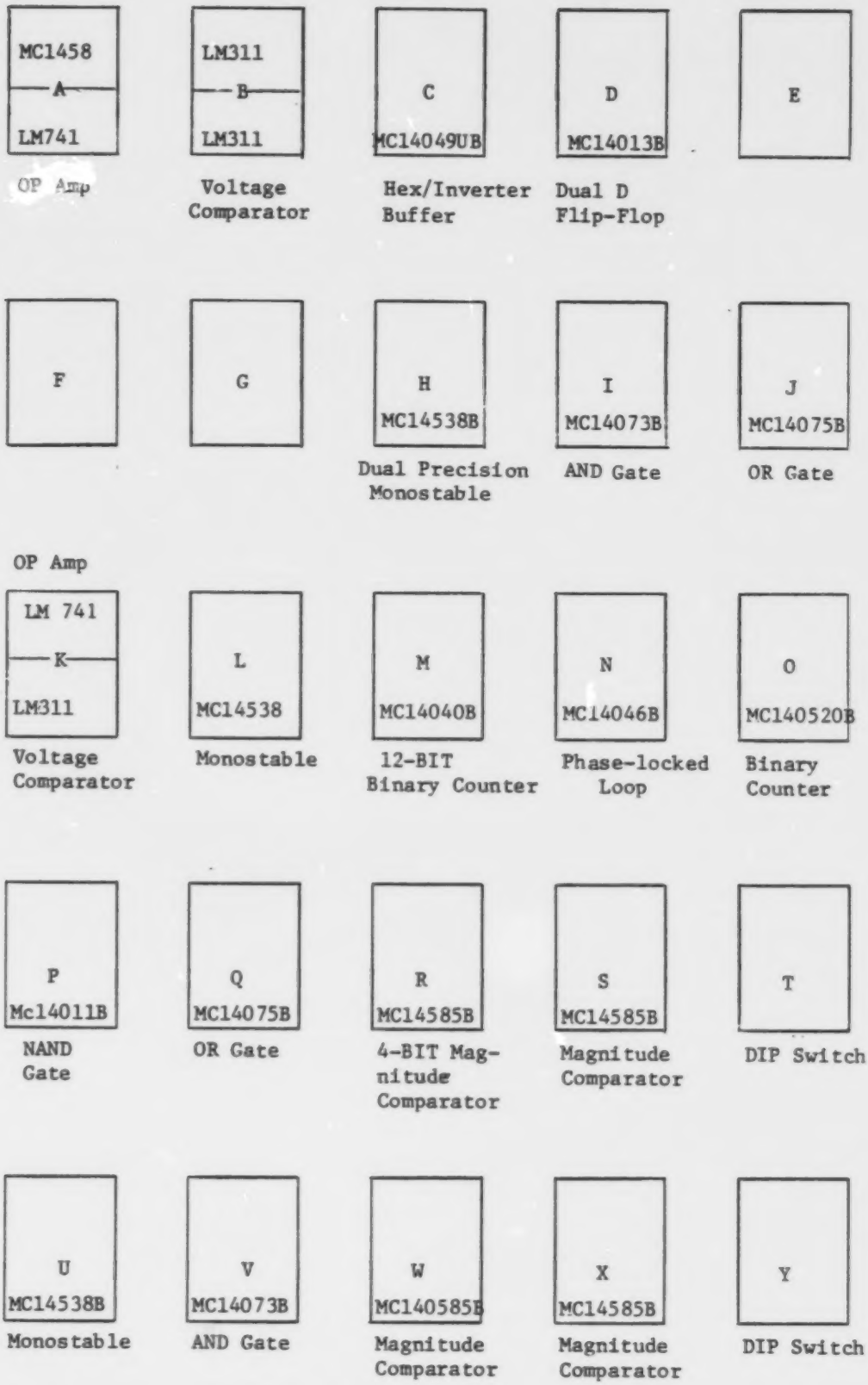


FIG. D8 SLIP RECOVERY LOGIC LAYOUT

called f_o, is directly proportional to the magnitude of input voltage at A8. The input signal at Q8 is the same as the final output at U10 (frequency divider output). Should the frequency of signals at U10, called $6f_e$, be more than or equal to f_o, i.e., the frequency of ramp pulses at K_t6, then no signals appear at L10 since the generated ramps at K_t6 would not have sufficient time to rise to the level ($\simeq$7.5V) necessary to trigger comparator K_b. In the case of $6f_e < f_o$ the input at Q8 serves as a resetting pulse synchronizing the generation of ramp pulses at K_t6 with the moment the output signal at U10 becomes "Low". The waveforms of Fig. D9 display the expected signals at different points of the break frequency oscillator when $6f_e < f_o$.

(2) Frequency Multiplier: The output of tachometer signal conditioning circuit, Fig. D5, appearing at D1 is the input to phase-locked loop N (Fig.D7) at its terminal 14. Chip N in conjunction with up counter O multiplies the frequency (zfm) of input signals at N14 by a number, called x, equal to a power of 2 ($x = 2^n$ with $n = 1, 2, 3, \ldots 8$). In Fig. D7 this number is shown to be 4. Fig. D10 demonstrates the expected waveforms of this part of the circuit.

(3) Motoring/Braking Mode Selection: The selection of motoring or braking mode of operation is determined by the outputs of dual NAND gate P in Fig. D7. For a motoring operation the input to A28 is "Low" while that of A29 is "High". In this case the output (m) at P10 would be "High" while that of P11 remains "Low". For a braking operation A28 and A29 become respectively "High" and "Low" which result in a "Low" (m) and a "High" ($\bar{m}$). The effect of a "High" (m) or ($\bar{m}$) on the operation of the slip recovery logic of Fig. D7 is explained in the following two parts.

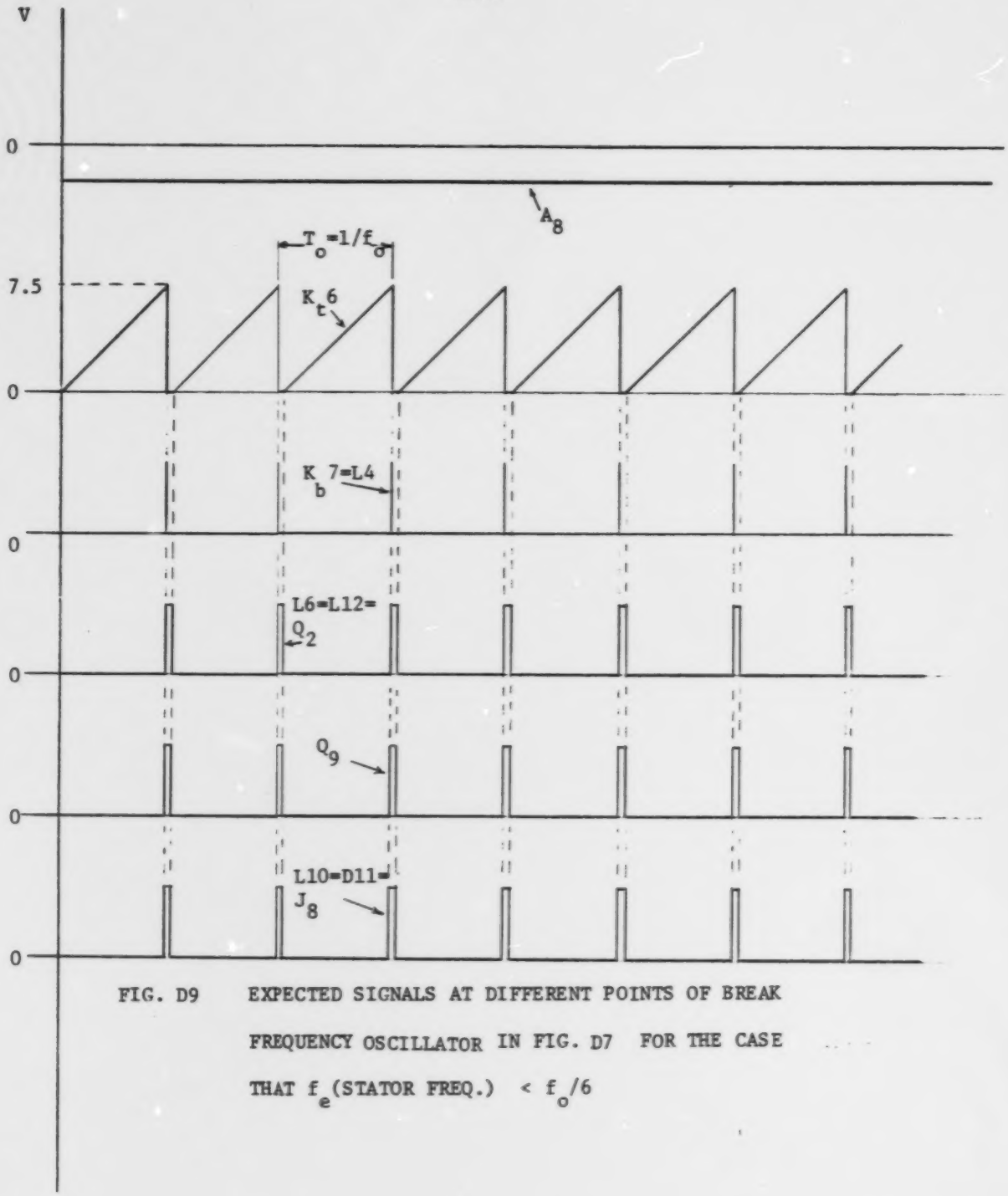


FIG. D9 EXPECTED SIGNALS AT DIFFERENT POINTS OF BREAK FREQUENCY OSCILLATOR IN FIG. D7 FOR THE CASE THAT f_e (STATOR FREQ.) $< f_o/6$

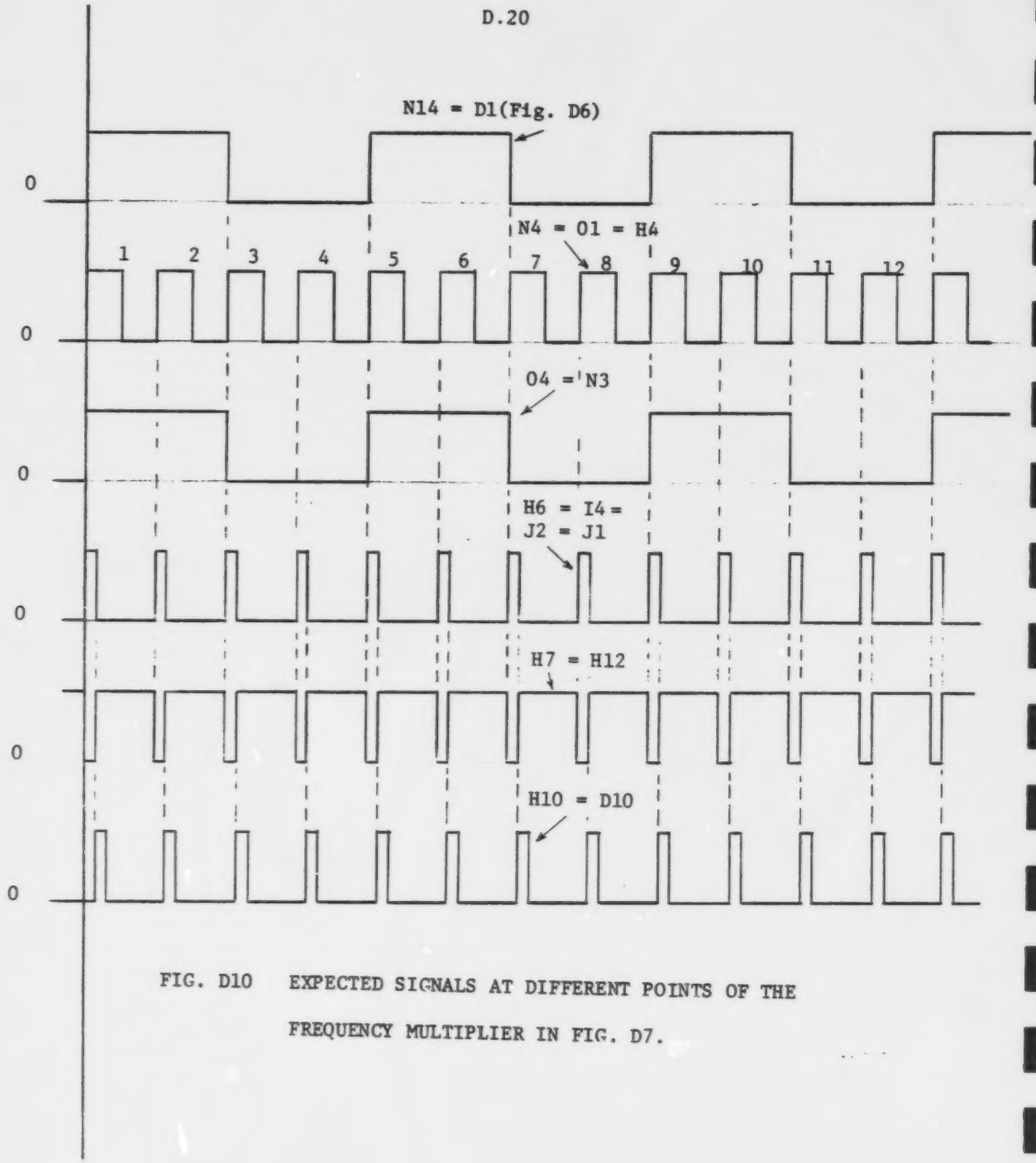


FIG. D10 EXPECTED SIGNALS AT DIFFERENT POINTS OF THE FREQUENCY MULTIPLIER IN FIG. D7.

(4) Frequency Addition (Motoring)/Subtraction (Braking): Depending on the mode of operation the logic circuit should perform the addition or the subtraction of two frequencies. The addition or subtraction of two frequencies is done in the following way. Monostable H receives square signals with a frequency equal to (xzf_m) at its terminal 4. The narrow pulses at H6 have the same frequency, i.e. xzf_m. The signals at H6 are added to the signals appearing at L10 by OR gate J shown at the upper right corner of Fig. D7. In this case the frequency of signals at J9 would be equal to $f_o + xzf_m$ (note that no pulses appear at L10 if the frequency of the final signals at U10 (X), called $6f_e$, is more than f_o. Now if m = 1 (motoring) then I9 = J9 and since I6 is "Low" the signals arriving at J6 would have a frequency equal to $xzf_m + f_o$. For a braking operation and for the case that there exist signals at L10, $\bar{m} = 1$ and the signals at I6 have a frequency equal to $xzf_m - f_o$. Fig. D11 shows the corresponding waveforms for a braking mode of operation. It is seen that D flip-flop D is reset by signals at H10 which have a frequency equal to xzf_m. The output signals at D13 then have the same frequency as those at D11, i.e., f_o. The output signals from D12 constitute one of the inputs to AND gate I. If I3 was always "High" then I6 would have a frequency equal to that of I4, i.e., xzf_m. However, I3 becomes "Low" with a frequency equal to (f_o) so that the resultant signals at I6 and J6 have a frequency equal to $xzf_m - f_o$.

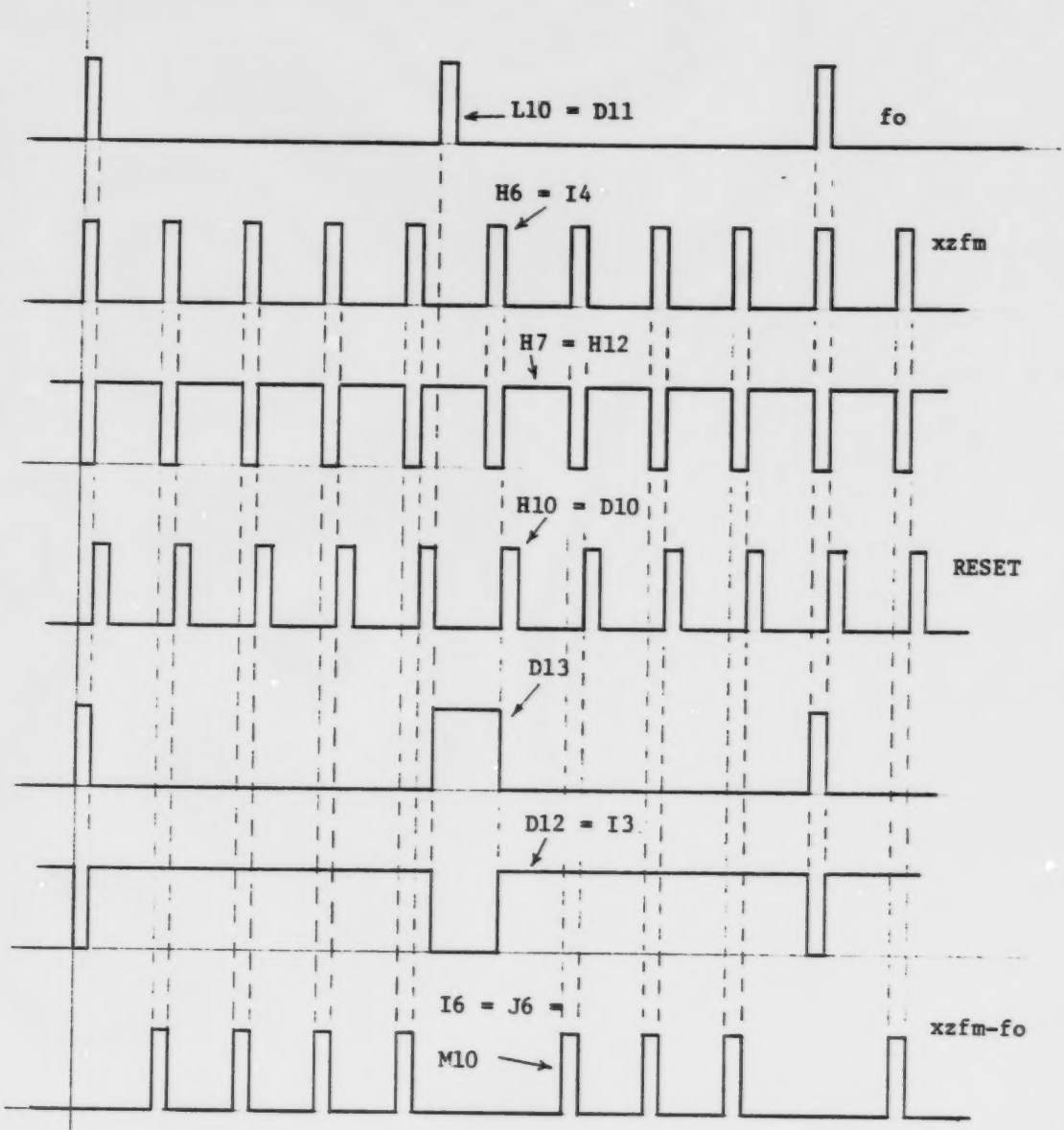


FIG. D11 FREQUENCY SUBTRACTION IN FIG. D7 FOR A BRAKING MOTOR OPERATION.

(5) Frequency Divider: The last part of slip recovery logic circuit of Fig. D7 is employed to divide the frequency of signals at J6 by a number determined by the positions of poles in either of dip switches T or Y. Each of these switches have seven poles and any pole depending on being open or closed represents a binary digit "0" or "1" so that the arrangement of poles in switch T or Y can represent a binary number from $(0000001)_2 = 1$ to $(1111111)_2 = 127$. In Fig. D7 chip M is a counter whose outputs are connected to magnitude comparators R and S in parallel with magnitude comparators W and X. If the logic output is used for a motoring mode ($m = 1$) then V9 becomes "High" as soon as the number of pulses received at M10 is the same as the number represented by the arrangement of the poles in switch T. In this event Q6 goes "High" and a narrow pulse appears at U10 (X). The pulse appearing at U10 after being inverted twice appears at terminal A36 which drives the inverter logic circuit as explained in the next part. The pulse at U10 (X) also resets counter M thus preparing it for counting the next series of pulses. Fig. D12 shows the corresponding expected signals for a motoring operation and for the case that the number represented by switch T is equal to $(0100111)_2 = 39$. For a braking mode ($\bar{m} = 1$) the division is done in the same way where the divisor is determined by the arrangement of poles in switch Y. In general, if the divisor is called (y) then the frequency of pulses reaching terminal A36 is equal to $6f_e = (xzf_m \pm f_o)/y$ where f_e is the output frequency of an inverter logic circuit driven by the signals at A36.

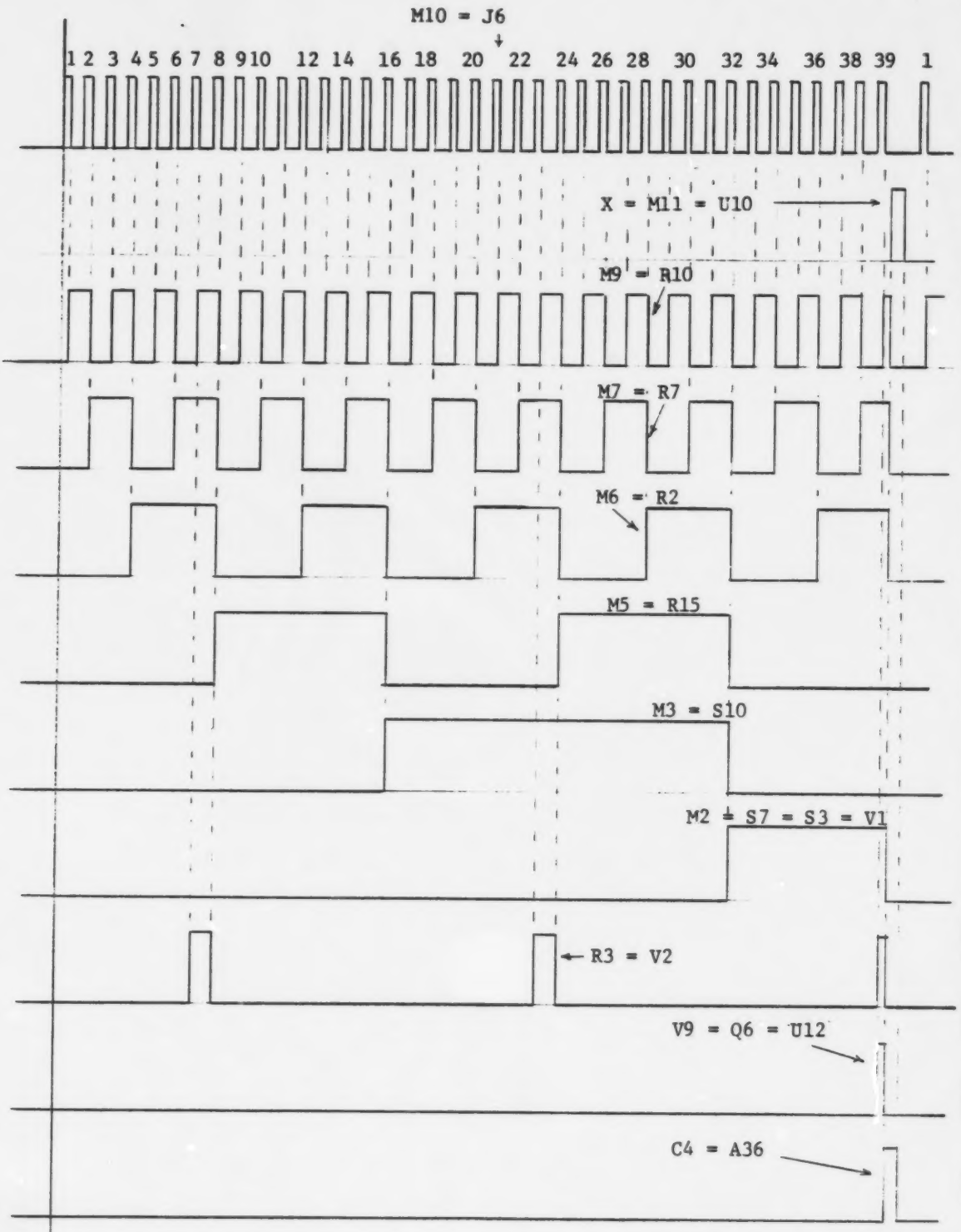


FIG D12 EXPECTED SIGNALS AT DIFFERENT POINTS OF FREQ. DIVIDER IN FIG. D7 FOR A MOTORING MODE (m = 1) AND FOR THE CASE THE INPUT FREQ. TO COUNTER M IS DIVIDED BY 39.

D3.2.3 Three-Phase Current Source Inverter Logic

The logic circuit shown in Fig. D13 is employed in gating the thyristors of a three phase current source inverter. The frequency of the output signals of this logic circuit can either be controlled locally by adjusting potentiometers P1-P3 or externally by closing switch S1 and exciting terminal 5 of NAND gate J with some signals. In this case the motor driven by the current source inverter whose thyristors are gated by the output signals of Fig. D13 (through pulse amplifiers) operates under a specific control strategy. For our case when the output of the slip recovery logic of Fig. D7, i.e., A36, is connected to J5 the motor would then operate with a constant slip if the stator frequency exceeds a predetermined value. The following is a detailed description of operation of Fig. D13 which can also be used in gating the thyristors of a single-phase (T_1, T_1, T_4, T_4) current source inverter power module. The circuit has also the feature of forward/reverse gating sequence. Fig. D14 illustrates a timing diagram of signals occuring in logic circuit of Fig. D13. The interface to the P.C. card of inverter logic and T_1 signal-reference logic employed in instrumentation are shown in Fig. D15. The IC chips layout along with their code numbers used for Fig. D13 are demonstrated in Fig. D16.

(1) Production of Inverter Clock: The squarewave waveform in Fig. D14 (I) is produced by the VCO subsection of "D". This clock frequency can be varied by adjusting the 1K potentiometer (P_2). The values of .015μfd capacitor and 27K resistor set the frequency available. The voltage limits of (P_2) are set by (P_3) and (P_1) for 6 Hz and 720 Hz respectively.

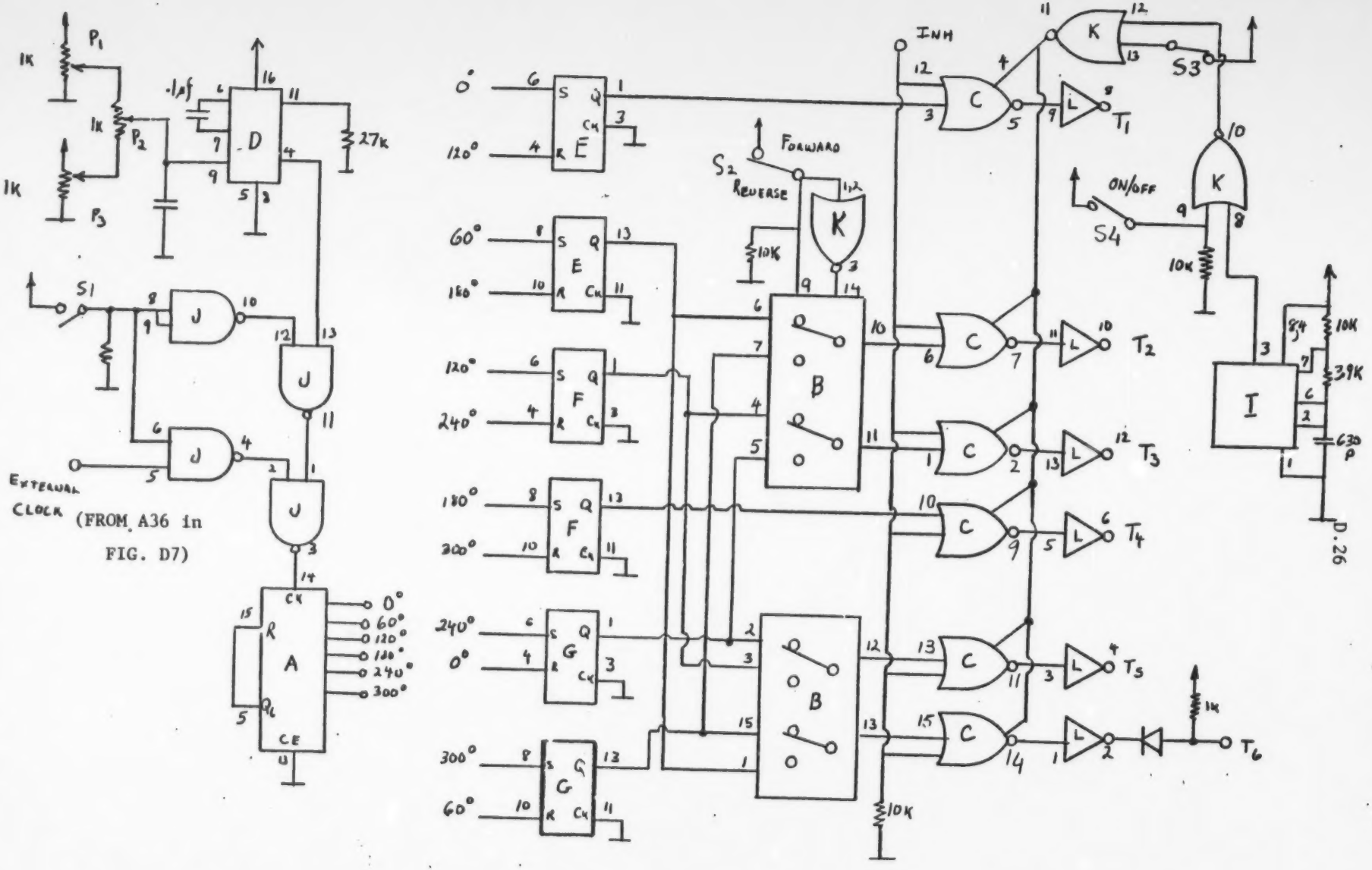


FIG. D13 3 PHASE CURRENT SOURCE INVERTER LOGIC

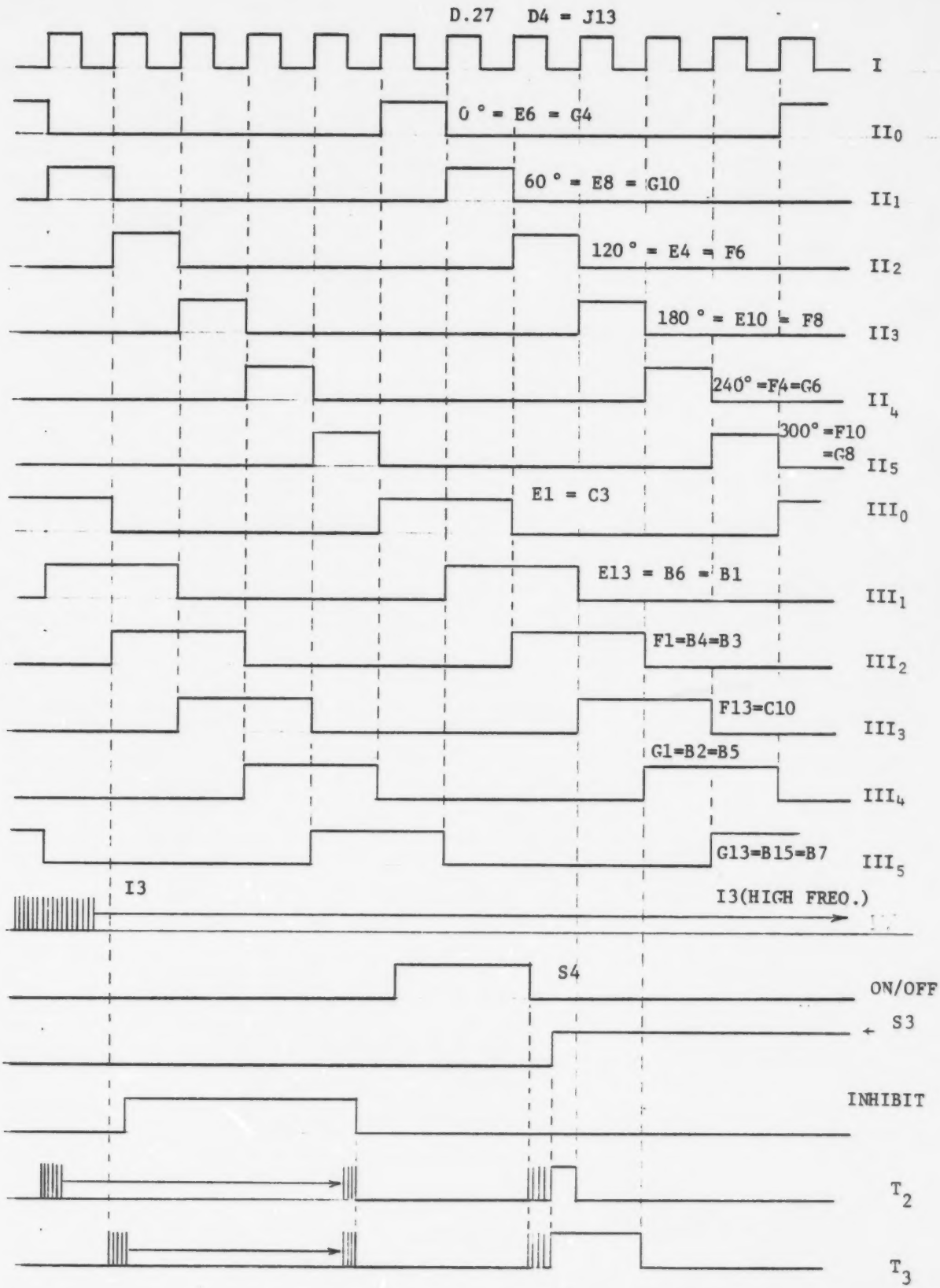


FIG. D14 TIME DIAGRAM OF CURRENT SOURCE INVERTER

LOGIC OF FIG. D13

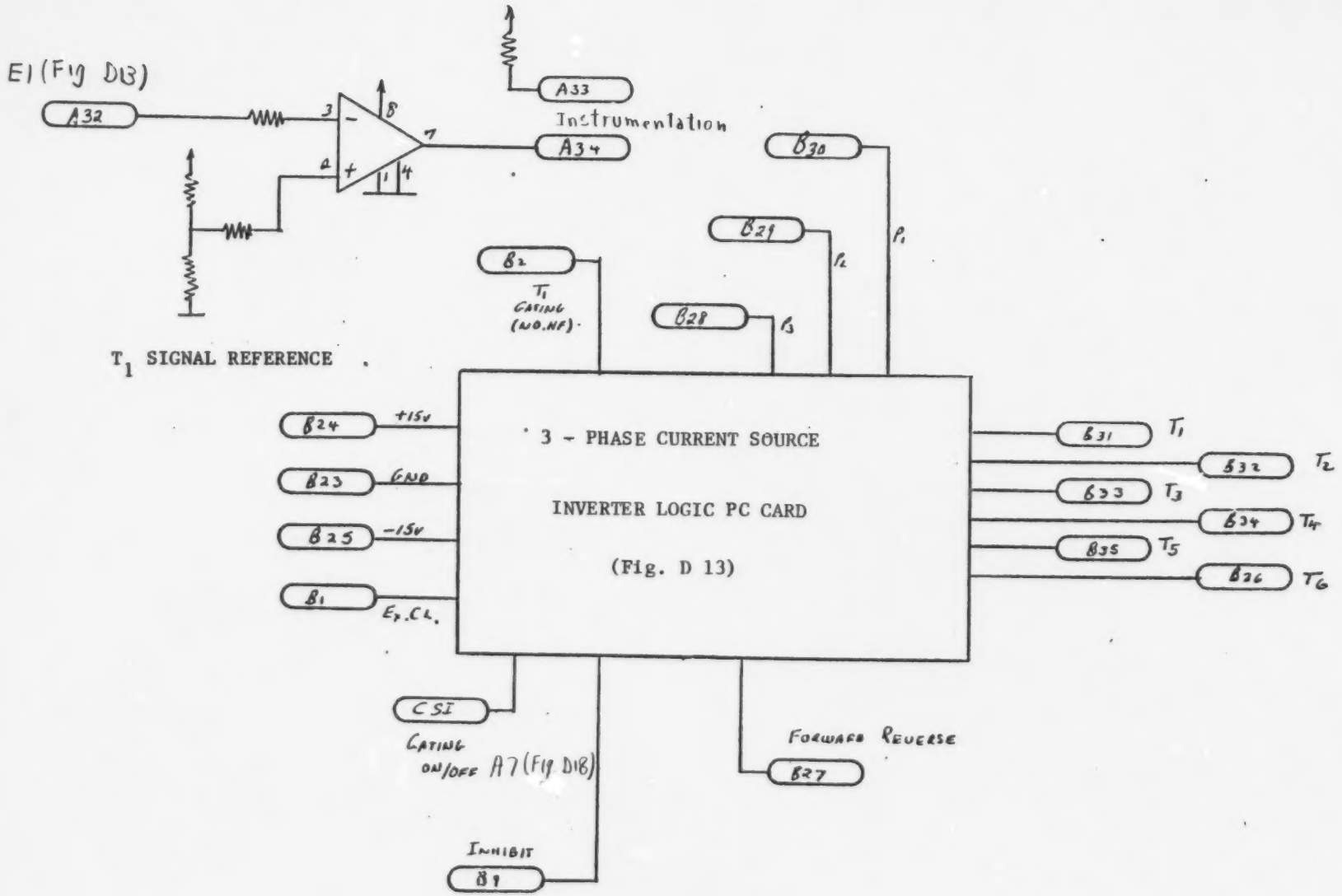


FIG. D15

INTERFACE TO CURRENT SOURCE INVERTER P.C. CARD AND T1 SIGNAL-REFERENCE LOGIC

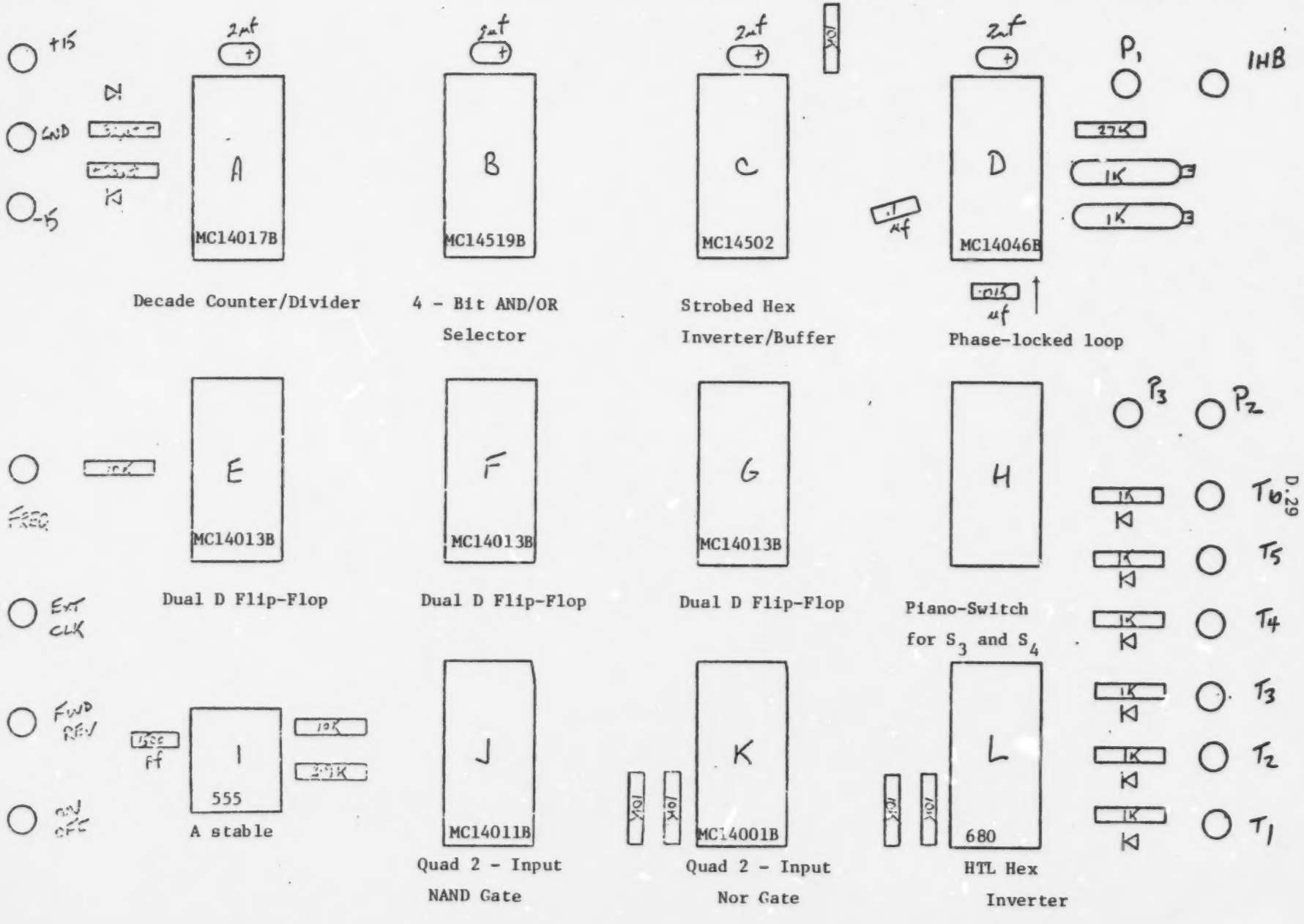


FIG. D16 CURRENT SOURCE INVERTER LOGIC LAYOUT

(2) External Clock Control: Switch S_1 and NAND gates J select VCO clock (already described) or an external clock for inverter operation. When S_1 is closed J-6 is 'High' allowing external clock at J-5 to appear inverted at J-4 . Also J-8,9 is 'High' forcing J-10 and J-12 'Low'. Therefore J-11 will be 'High' regardless of signal at J-13. If Switch S_1 is left open J-6 is 'Low' and VCO clock appears at J-3.

(3) Frequency Division: The clock signal (J-3) advances decade counter A one step each clock pulse producing waveforms shown in Fig. D14 (II_N). The sixth clock pulse produces an output at A-5 which resets the counter at A-15. The counter therefore does not count a decade but repeats output waveforms every six clock pulses. Counter A outputs are labelled 0^o, 60^o, etc., representing points in time of one inverter cycle.

(4) 120^o Gating: SR flip-flops E, F, & G are set and reset from the counter outputs to produce the 120^o waveforms shown in Fig. D14 (III_N). Specifically, E-6 receives a pulse, Fig. D14 (II_o), at 0^o setting E-1 to 'High' (shown in Fig. D14 by (III_o)). E-4 receives a pulse, Fig. D14 (II_2), at 120^o resetting E-1 to 'Low'.

Similarly other flip-flops produce waveforms, Fig. D14 (III_1, III_2, III_3, III_4, III_5).

(5) Forward/Reverse: The 3 phase inverter output sequence can be reversed by exchanging T_2 with T_6 and T_3 with T_5. Switch S_2 and gate K provide proper control for 4 bit selector B. When S_2 is closed B-9 is 'High' and B-14 'Low 'operating selector Switch B as shown in Fig. D13 for forward phase direction. Opening Switch S_2 changes selector Switch B to reverse phase direction.

(6) High Frequency Carrier: A stable Multivibrator "I" produces high frequency pulses as shown in Figure D14 (IV). The frequency (about 30 KHz) and duty cycle (2/3 'High') can be adjusted with resistors 10K, 3.9K and capacitor 630 pf.

This signal from "I-3" is inverted by K-10 when switch S_4 is 'Low'. If S_4 is 'High', K-10 remains 'Low' regardless of K-8.

The signal from K-10 is again inverted by K-11 to drive the disable input of strobed buffer C-4. With C-4 'Low' inverting gates C drive output gates L with 120° waveforms from Fig. D14 (III_N).

For normal operation the high frequency carrier disables buffer C and all outputs C-5, 7, 2, 9, 11, 14 are 'High Impedance' (see CMOS Data Book). With high impedance input to gates L outputs are all low (T_1, T_2, T_3, T_4, T_5, T_6).

If S_4 is switched 'High' (Logic 'Off') then disable is continuously high and $T_1 \ldots T_6$ are turned off.

(7) Transistor Gating: If S_3 is switched 'High' K-11 is always low and outputs $T_1 \ldots T_6$ appear like Fig. D14 (III_N) without high frequency carrier. This type of output could be used for a transistor inverter power circuit.

(8) Inhibit: If "Inhibit" C is connected 'High', 120° waveforms are bypassed and $T_1 \ldots T_6$ are all on (with high frequency carrier).

D3.2.4 Inverter Output Overvoltage Protection

The inverter protection against any overvoltage at its output terminals is provided by the circuit of Fig. D17. The output terminals of the inverter are connected to a full-wave bridge rectifier whose DC output voltage is proportional to the inverter output voltage. A part of this DC voltage, through 10K potentiometer, is compared with a reference voltage adjustable by a 5K potentiometer. As long as the inverter output voltage has not exceeded a predetermined value the terminal 7 of the comparator stays "High" which results in the conduction of the transistor and making terminal 6 of this transistor "Low". This terminal is connected to the "Inhibit" input of the inverter logic shown in Fig. D13. In the event of an overvoltage across inverter terminals the output of the comparator in Fig. D17 becomes "Low" thus turning off the transistor and making terminal 6 of the output "High" which shuts off the inverter gating signals.

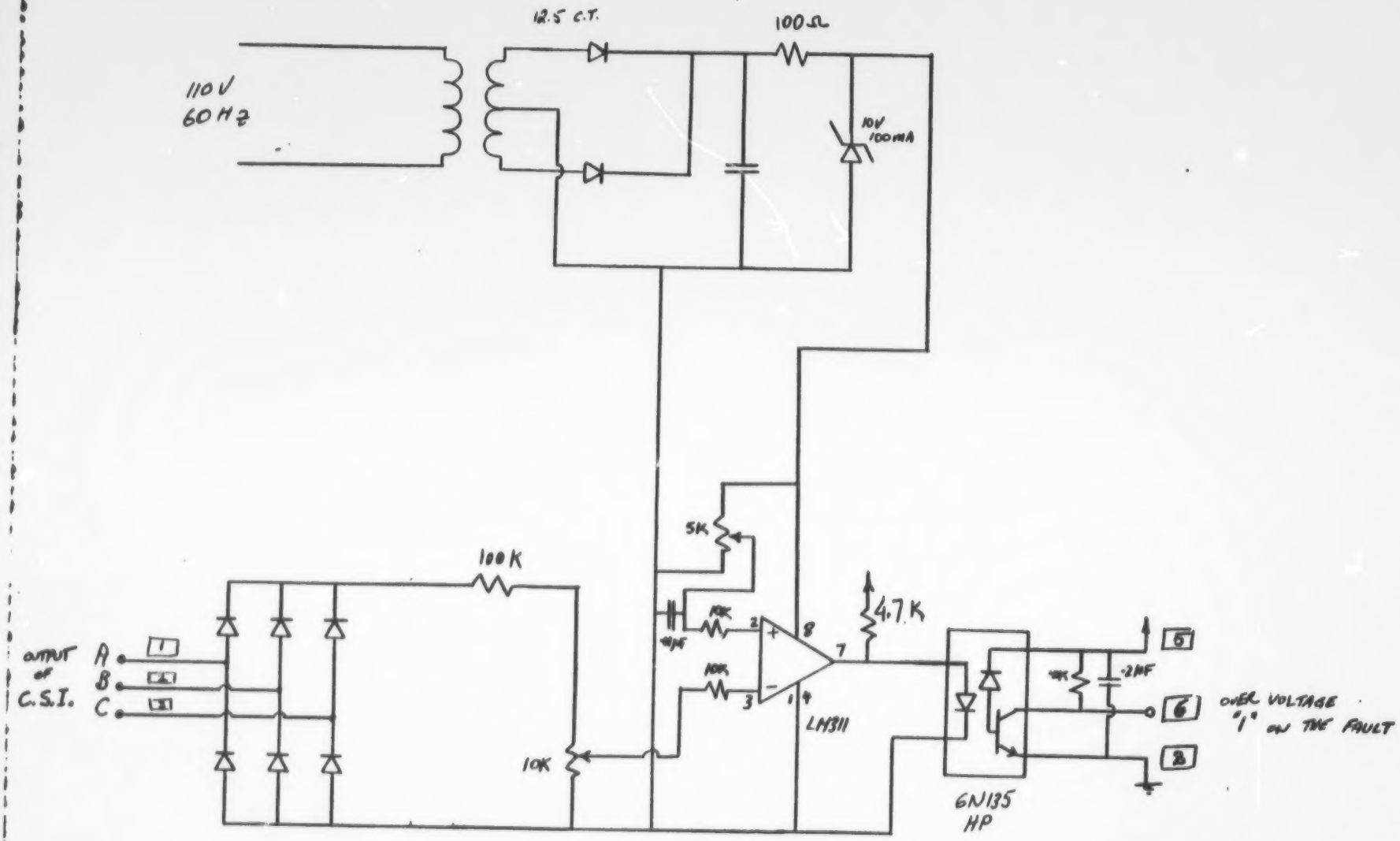


FIG. D17 CURRENT SOURCE INVERTER OUTPUT OVER VOLTAGE PROTECTION CIRCUIT

D3.2.5 Start/Stop Logic

The star/stop logic circuit shown in Fig. D18 is used for starting and stopping the generation of gating signals in Fig. D13 (shown by switch S_4). For starting A6 in Fig. D18 goes "High" thus setting the D flip-flop D shown in this figure (equivalent to the "OFF" position of switch S_4 in Fig. D13). When A5 in Fig. D18 goes "High" the flip-flop is reset and no gating pulses are produced (equivalent to the "ON" position of switch S_4 in Fig. D13.

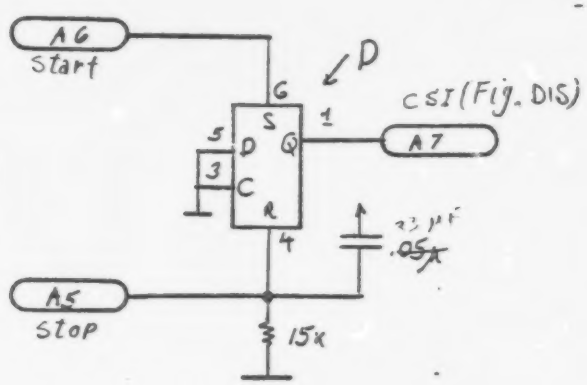


FIG. D18 START/STOP LOGIC

D 3.2.6 Pulse Amplifier

The logic signals $T_1 \ldots T_6$ produced by the logic circuit of Fig. D13 are the inputs to pulse amplifiers. The pulse amplifier by definition amplifies the logic signals (pulses) to provide sufficient current and voltage to ensure solid thyristor turn-on. Device manufacturers recommend a 20 volt O.C. source with 20Ω impedance and with a risetime less than 100ns for failure free turn-on. In the following the operation of a pulse amplifier using VMOS transistor is explained. This design can provide 1 amp current from a 28 volt supply with a risetime less than 20NS*.

VMOS Implementation: The 'VN46AF' (Siliconix) power FET is rated at

- 40 Volts Maximum Drain-Source
- 2 amps Maximum Drain Current
- * - 5NS Maximum Switching Time
- 100 MA Maximum Reverse Gate Current
- 150°C Maximum Operating
- 3.0 Volts Maximum V_{DS} @ 1 amp Drain Current
- 100μA Maximum Forward Gate Leakage

This high speed switch well suits the very simple digital amplifier design shown in Fig. D19. 'R_1' ensures that the input gate will not turn on with noise or a high impedance input signal. The logic signal output stage, Fig. D20, will pull the input high [$I_{IN} = 30\ (R_1 + R_3) = 2.7$ MA, $V_{IN} = I_{IN} \cdot R_1 - 15 = 12.27$ volts]. R_2 prevents excessive current in the event of output short circuit [$I_{SHORT} = (V_{28} - V_{OS_{SAT}}) / R_2 = 830$ MA]. Fast recovery diode D protects switch VN from high voltage by providing a path for inductive energy stored in load. Capacitors C_1 and C_2 filter high frequency ripple which would otherwise be fed back to main supply and possibly interfere with other circuits. Table D2 gives the list of components necessary for constructing six pulse amplifiers.

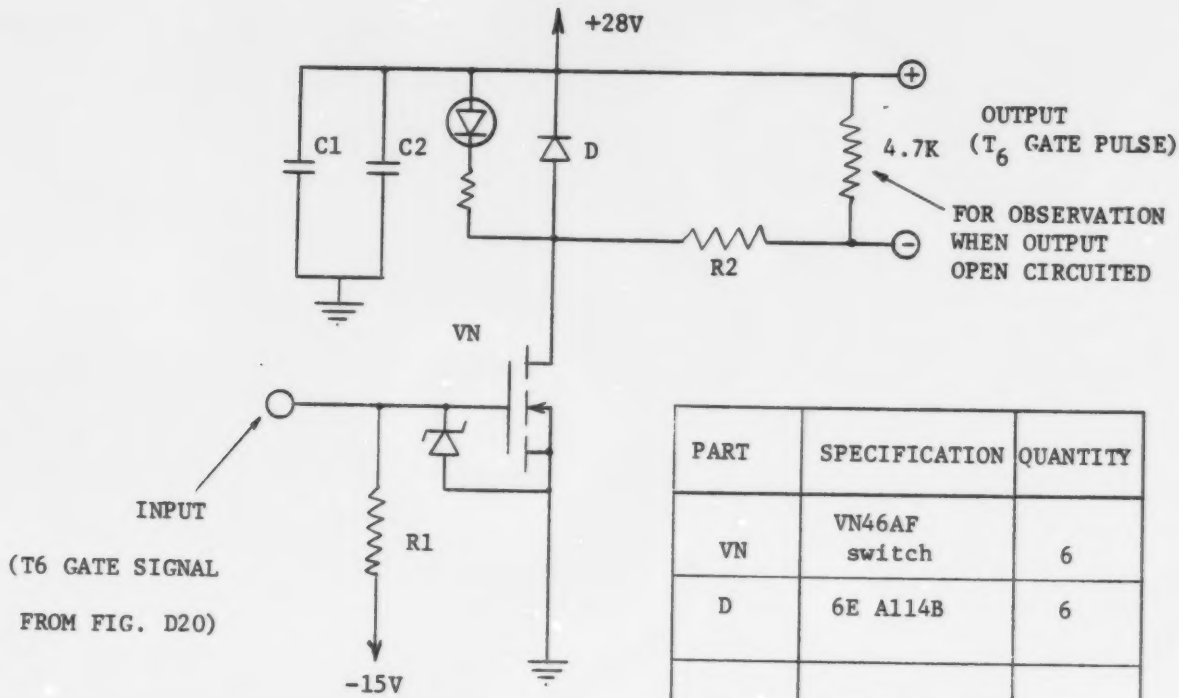


FIG. D19 DIGITAL PULSE AMPLIFIER USING VMOS TRANSISTORS (SHOWN ONLY FOR T_6)

PART	SPECIFICATION	QUANTITY
VN	VN46AF switch	6
D	6E A114B	6
C_1	400μfd,25V	1
C_2	.1μfd,50V	2
R_1	10K, 1/4W	6
R_2	30Ω,10W	6

TABLE D2 PARTS LIST FOR SIX PULSE AMPLIFIERS

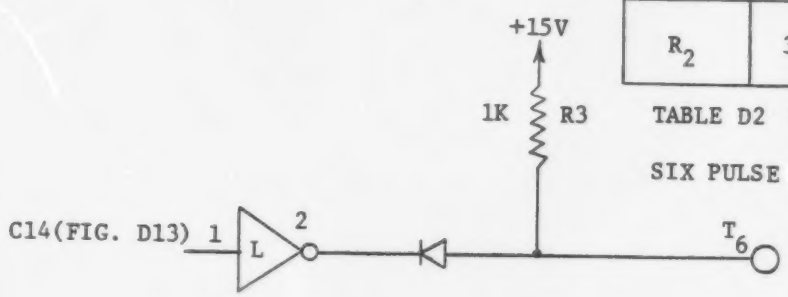


FIG. D20 LOGIC OUTPUT STAGE 'PASSIVE PULL UP' (SHOWN ONLY FOR T_6)

D3.2.7 Logic Layout and Connections

The layout of logic P.C. cards, logic power supply and pulse amplifiers along with their corresponding connectors are shown in Fig. D21. P.C. board (1) consists of logic circuits of tachometer signal conditioning (Fig. D5) and slip recovery (Fig. D7). P.C. Board (2) constitutes the inverter logic circuit of Fig. D13. The connections/interconnections of the connectors shown in Fig. D21 are given in Tables D3 to D8. Table D3 displays the connections of connector (A) of the slip recovery and tachometer signal conditioning P.C. card (board 1) and those of connector (B) of the inverter logic P.C. card (board 2). Table D4 gives the interconnections of connectors (A) and (B). The connections of the main terminal strip connector, L, are shown in Table D5 while Table D6 gives the details of the interconnections between main terminal strip connector (L) and connectors (A) and (B). The interconnections between the main terminal strip connector, L, and the power circuit are demonstrated in Table D7. The last table (D8) gives the particulars of the control panel of phase control. Finally, Figs. D22-D24 show respectively the pulse amplifier wiring, logic power supply terminals and front panel wiring.

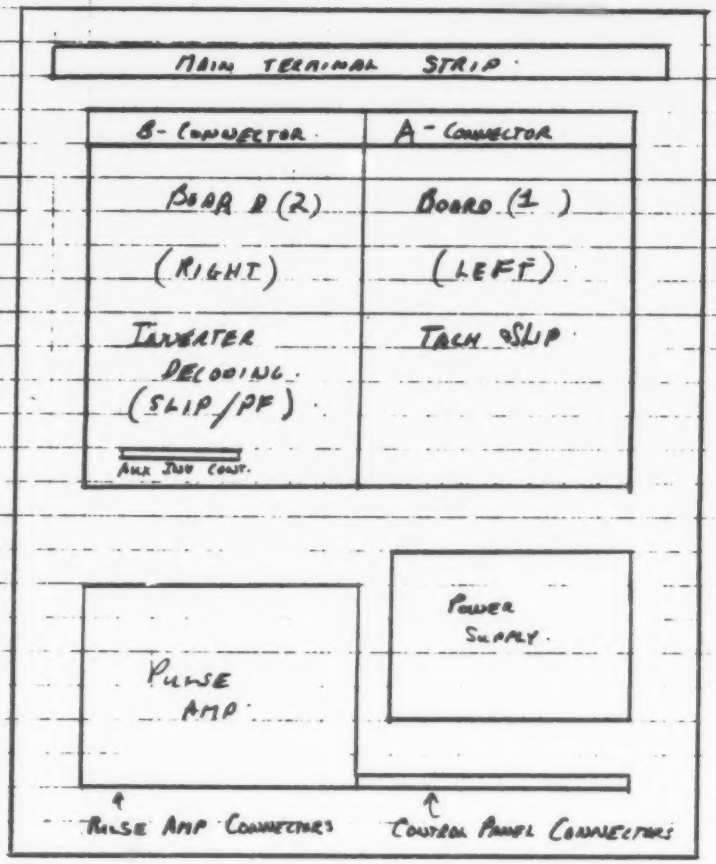


FIG. D21 LOGIC LAYOUT

Slip		Inv.	
A1		B1	VCO IN
2	TACH INPUT	2	T1 GATING SIGNAL (NO HF)
3		3	ON/OFF
4		4	POWER FACTOR INPUT
5	OVERVOLTAGE IN	5	VOLTAGE
6	" OUT	6	
7	" RESET	7	
8	POT INPUT (SLIP)	8	
9		9	INHIBIT - OVER VOLTAGE (Normally 0)
10		10	
11		11	MANUAL/AUTO
12	-15 I (IN)	12	
13		13	
14		14	
15		15	
16		16	
17	USED FOR RAILS	17	
18		18	
19		19	
20		20	USED FOR RAILS
21		21	
22		22	
23	GND	23	GND
24	+15V (IN)	24	+15
25		25	-15V
26		26	
27		27	FORWARD
28	(MOTORING	28	P3
29	BRAKING)	29	P2
30		30	P1
31		31	T1
32	FROM T1 GATING SIGNAL	32	T2
33	OPTICALLY COUPLED	33	T3
34	T1 GATING REFERENCE	34	T4
35		35	T5
36	VCO OUT	36	T6

TABLE D 3 AUGAT BOARD CONNECTOR

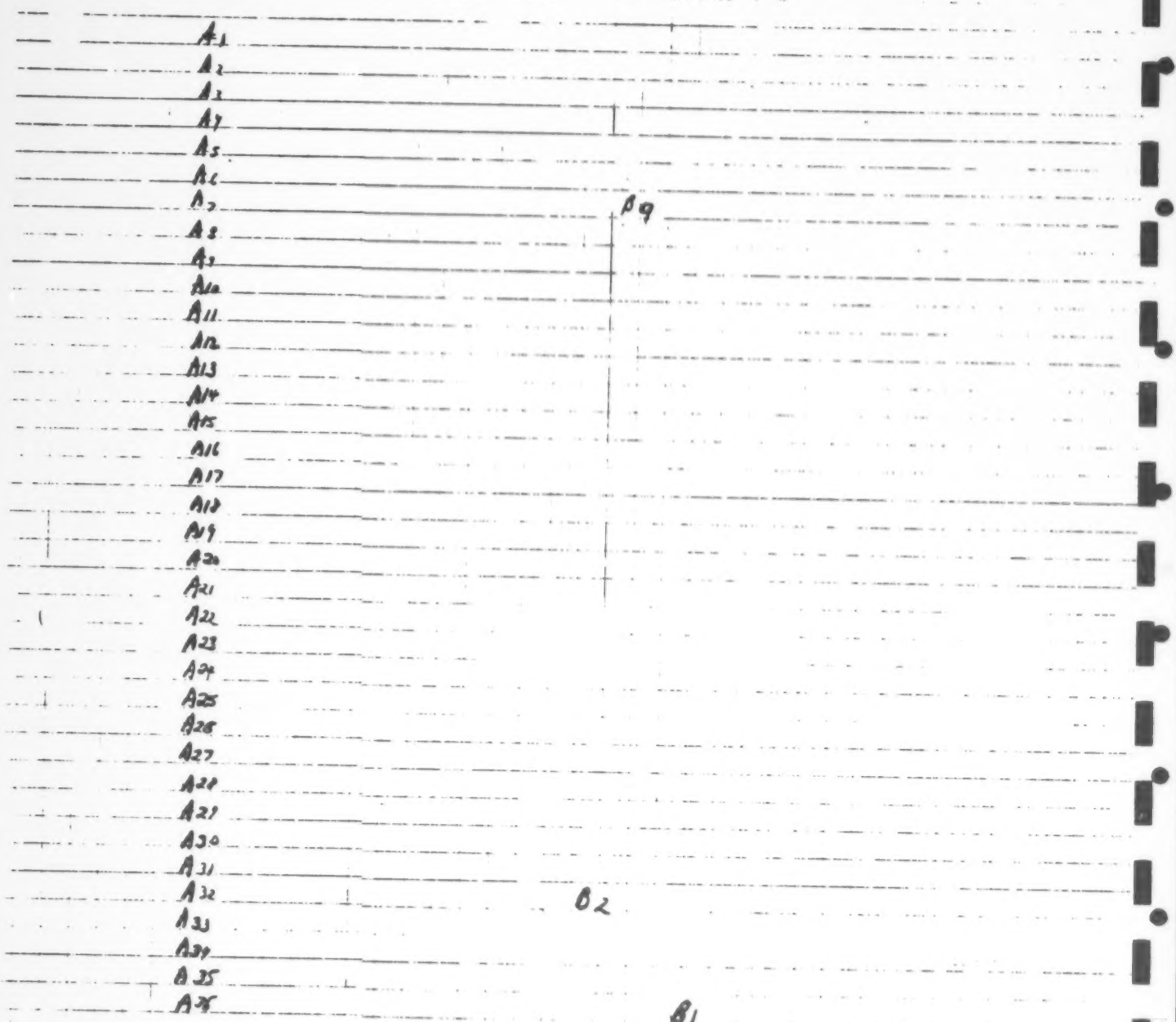


TABLE D 4 INTERCONNECTION OF AUGAT BOARDS

1	L_1	110 V AC
2		
3		TALK INPUT
4		
5		
6		MOTOR / BRAKING
7		
8		POWER FACTOR
9		INPUT VOLTAGE
10	RESET	$-M_7$
11	+15V	$-M_9$
12	GND	$-M_1$
13	-15V	$-M_3$
14	Pot for slip fo	$-M_2$
15	optically coupled current reference	
16		
17		
18		
19		
20		
21		
22	OVERVOLTAGE SIGNAL.	
23	ON/OFF (GATING)	M-8
24		
25		
26		
27		
28	MANUAL/AUTO	
29		
30		
31	FORWARD / REVERSE	
32	P_3	
33	P_2 (V(0 - POT)	
34	P_1	
35	T_1	
36	T_2	
37	T_3	
38	T_4	
39	T_5	
40	T_6	

TABLE D 5 MAIN TERMINAL STRIP CONNECTOR "L"

L_1	S_1
2	S_2
3	
4	
5	
6	
7	
8	P_{39}
9	P_{40}
10	
11	S_4
12	S_5
13	S_6
14	
15	
16	
17	
18	
19	
20	
21	
22	P_{13}
23	
24	
25	
26	
27	
28	
29	
30	
31	
32	
33	
34	
35	P_{21}
36	P_{24}
37	P_{27}
38	P_{30}
39	P_{33}
40	P_{36}

TABLE D 6 INTERCONNECTION OF MAIN TERMINAL STRIP TO AUGAT CONNECTORS

L1	1
2	
3	A1
4	A2
5	A3
6	A28
7	A29
8	B4
9	B5
10	A5
4	A24 , B24
12	A23 , B23
13	A22 , B25
14	
15	A33
16	A34
17	
18	
19	
20	
21	GND (L12)
22	A6
23	B3
24	
25	
26	
27	
28	B11
29	B12
30	
31	B27
32	B28
33	
34	
35	B31
36	B32
37	B33
38	B34
39	B35
40	B36

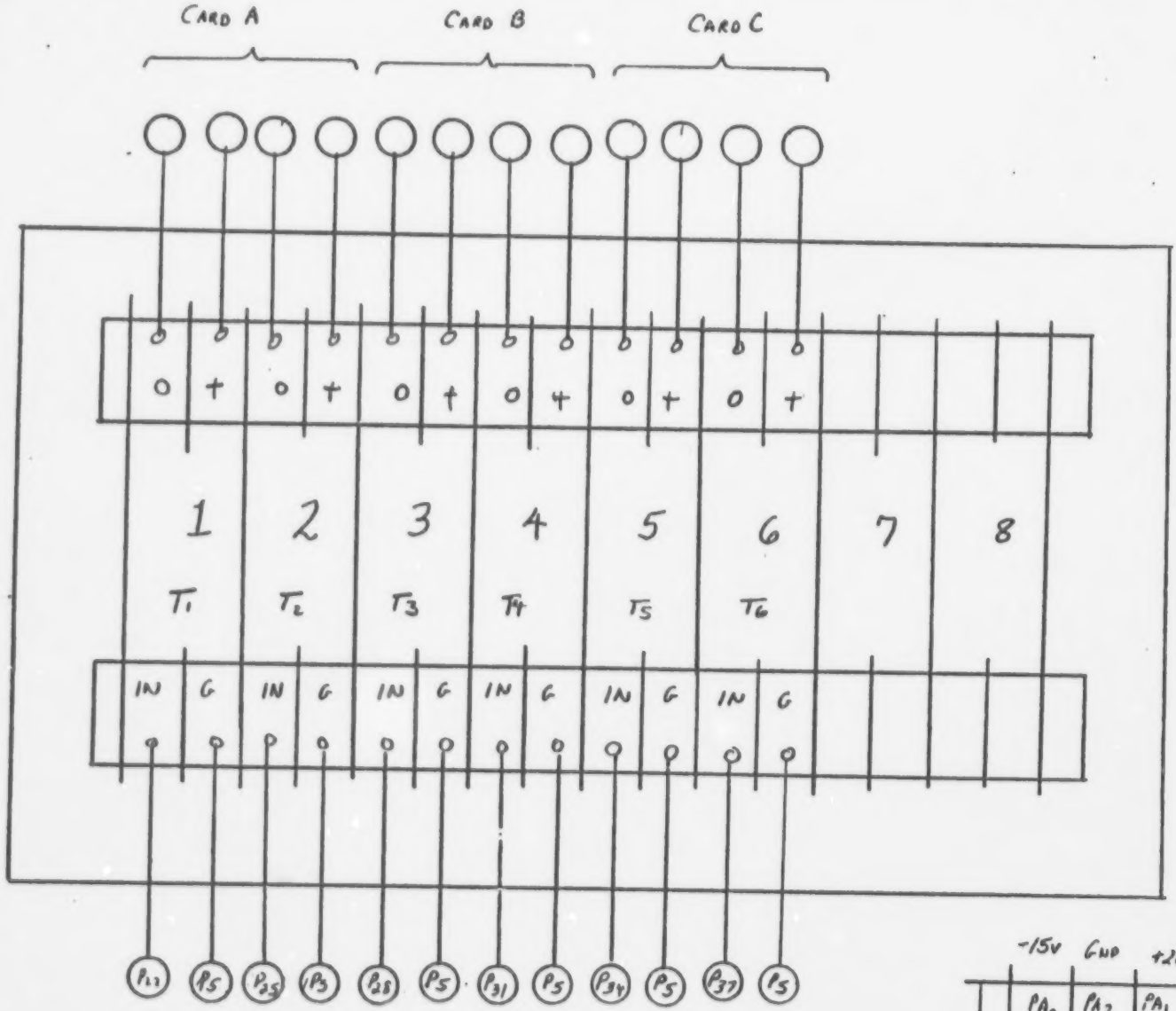
TABLE D7 INTERCONNECTION OF MAIN TERMINAL STRIP TO POWER CIRCUIT

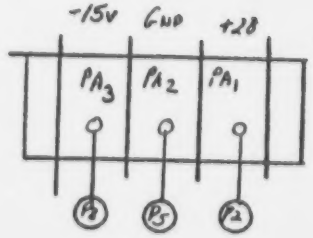
P21	L35
P22	IN-1
P23	
P24	L36
P25	IN-2
P26	
P27	L37
P28	IN-3
P29	
P30	L38
P31	IN-4
P32	
P33	L39
P34	IN-5
P35	
P36	L40
P37	IN-6
P38	
P39	L8
P40	L9

TOP

P1	S8	+28V
P2	PA1	
P3		
P4	S5	GND.
P5	PA-2	
P6		
P7	S6	-15V
P8	PA-3	
P9		
P10	S4	+15V
P11		
P12		
P13	L22	0V. SIGNAL
P14	0.V. SIGNAL	
P15		
P16		
P17		
P18		
P19		
P20		

Table D8 CONTROL PANEL OF PHASE CONTROL





BACK POWER SUPPLY.

FIG. D22 PULSE AMPLIFIER WIRING

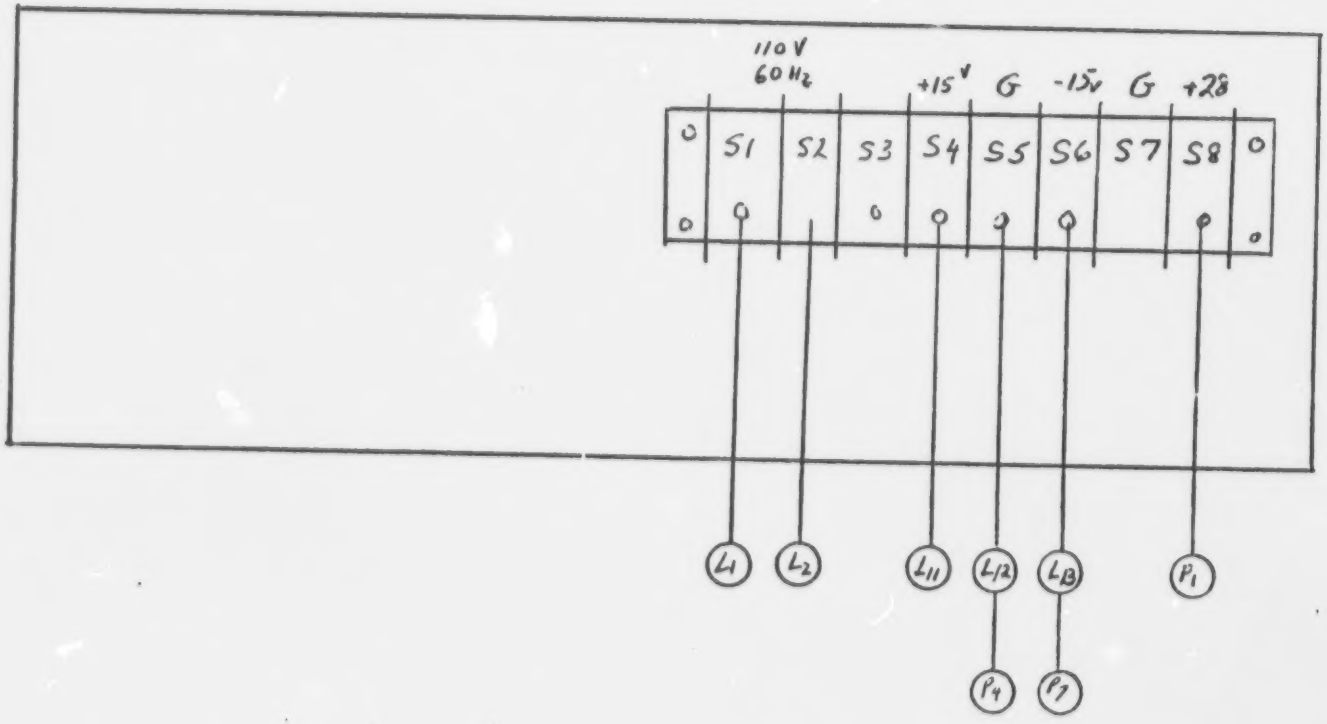


FIG. D23 POWER SUPPLY TERMINALS - SLIP RECOVERY LOGIC

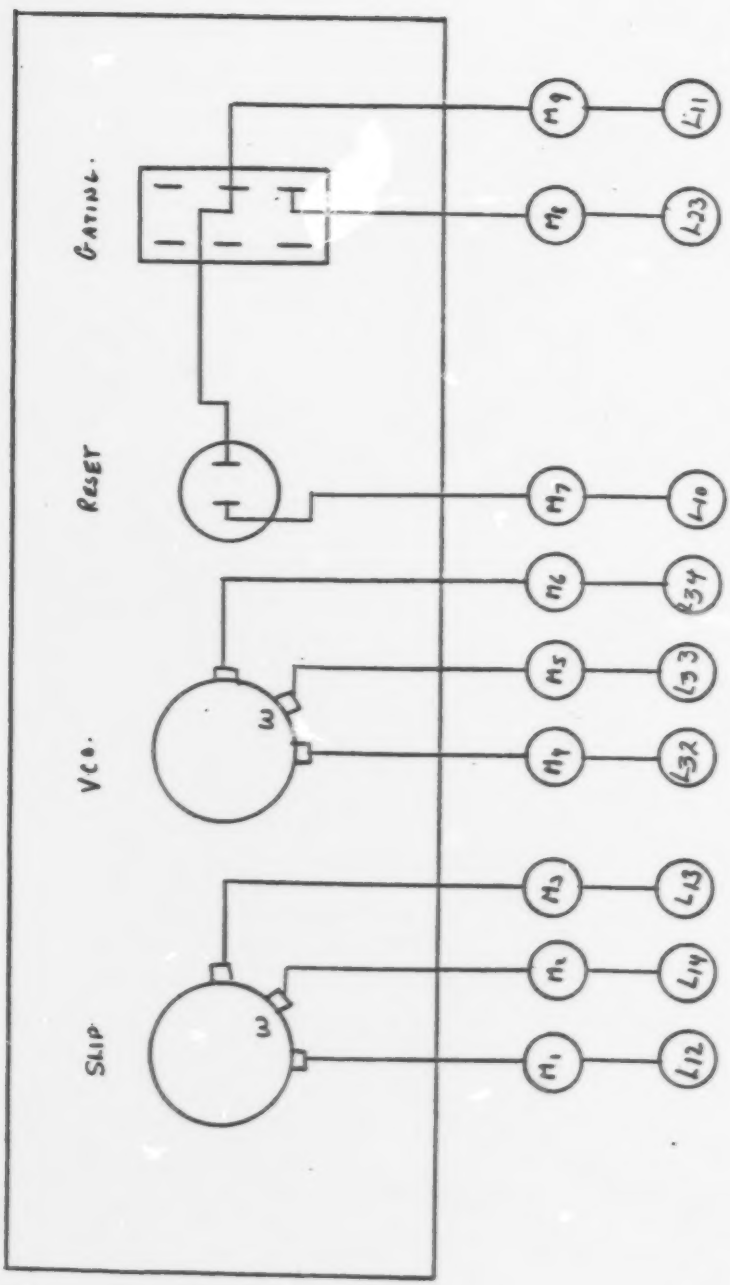


FIG. D24: FRONT PANEL WIRING - SLIP FEEDBACK SYSTEM

D3.3 Determination of Slip

The block diagram of Fig. D25 demonstrates the basics of the slip-control motor operation. The symbols used in this figure are:

f_o = Break frequency generated by section (1) in Fig. D7.

$x = 2^n (n = 1, 2, 3, \ldots 8)$ = Multiplication factor determined by section (2) in Fig. D7.

m = 1 = Motoring operation determined by sections (3) and (4) in Fig. D7.

$\bar{m}$ = 1 = Braking operation determined by sections (3) and (4) in Fig. D7.

y = 1, 2, 3...127 = Division factor determined by section (5) in Fig. D7.

f_m = Rotor rotational frequency.

z = Ratio of frequency of tachometer output signals to (f_m). This number depends on the tachometer construction.

f_e = Frequency of output signals of inverter logic circuit (Fig. D13).
= Motor stator frequency.

p = Motor number pair of poles.

The value of (f_o) is determined in the following way. The generated ramp pulses at K_t6 in section (1) of Fig. D7 have magnitudes equal to:

$$V_{kt6} = -\frac{1}{15\times10^{3}\times4.7\times10^{-9}}\int_{o}^{t} V_{a8}dt = \frac{-V_{a8}}{70.5\times10^{-6}}\,t \qquad V \qquad (1)$$

where V_{a8} is a negative voltage at terminal A8. Comparator K_b is triggered if V_{kt6} becomes almost equal to 7.5 V. In this case narrow pulses with a frequency equal to (f_o) appear at L10.

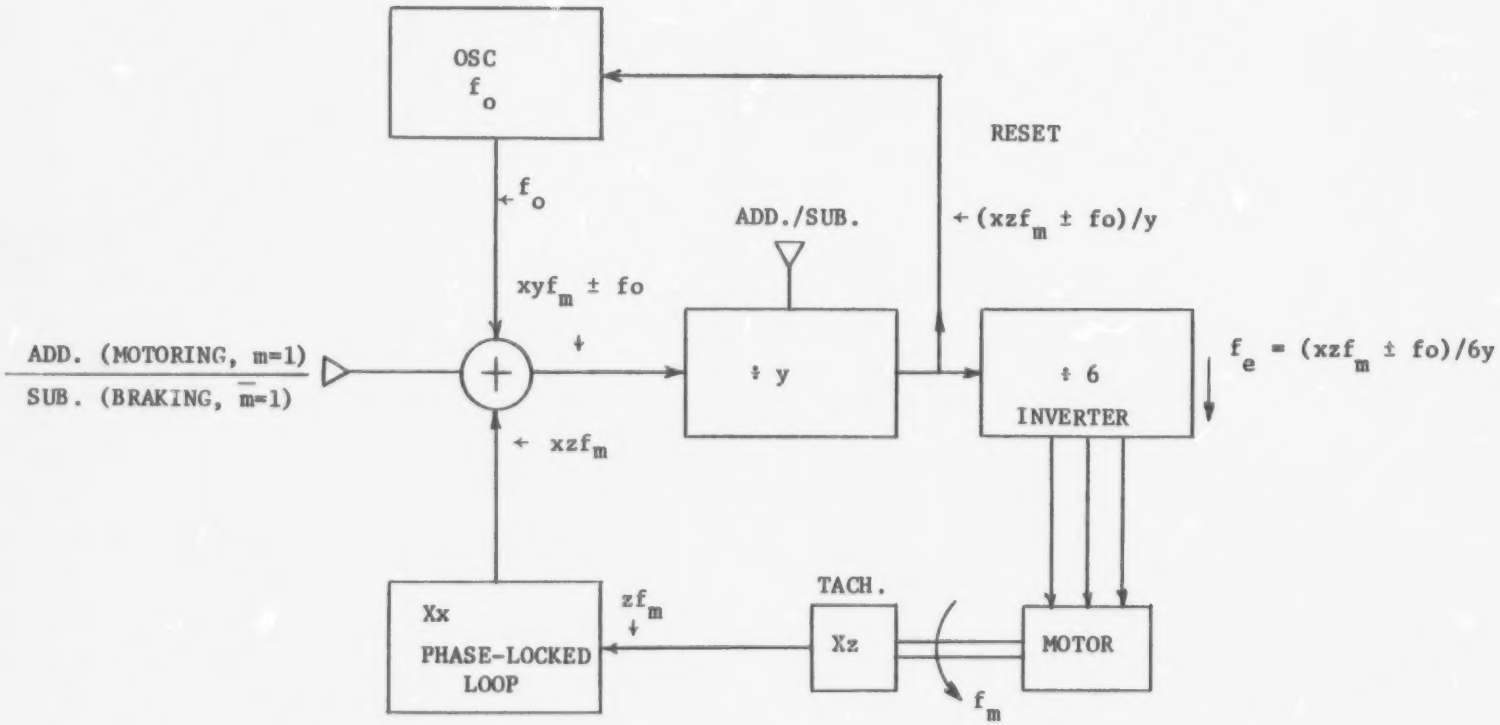


FIG. D25 BLOCK DIAGRAM OF MOTOR SLIP-RECOVERY OPERATION.

$$f_o = \frac{-V_{a8} \times 10^6}{528.75} \quad \text{Hz} \qquad (2)$$

For example, if $V_{a8} = -1$ V then,

$$f_o = 1891.25 \quad \text{Hz}$$

However, if the ramp pulses at $K_t 6$ fall to zero before reaching to the level necessary for triggering comparator K_b then no pulses appear at L10 and $f_o = 0$.

The relationships existing between variables of block diagram of Fig. D25 are:

$$f_s = \frac{f_e}{p} \qquad (3)$$

$$s = \frac{f_s - f_m}{f_s} = \frac{f_e - pf_m}{f_e} = 1 - \frac{pf_m}{f_e} \qquad (4)$$

where f_s and s are respectively the motor synchronous speed and slip. If $6f_e < f_o$ then

$$f_e = \frac{xzf_m \pm f_o}{6y} \qquad (5)$$

$$s = 1 - \frac{6ypf_m}{xzf_m \pm f_o} \qquad (6)$$

where (+) sign denotes a motoring mode of operation and (-) sign is used for a regenerating mode of operation. If $6f_e > f_o$, irrespective of motoring or regenerating, we have

$$f_e = \frac{xzf_m}{6y} \qquad (7)$$

$$s = 1 - \frac{6yp}{xz} \tag{8}$$

From Eq. (8) it yields,

$$y = \frac{xz(1-s)}{6p} \tag{9}$$

The above expression helps us in determining the multiplication and division factors, x and y, for any specific application where p, z and s are known values. In this respect $x = 2^n$ (with n = 1, 2,...8) should be chosen such that the resultant value of (y) from Eq. (9) be an integer between 1 to 127. Note that for a motoring mode (s) is positive while in a regenerating case it has a negative value. Table D9 gives examples for a few cases.

CA1
DTC 801
80
R22
c.2

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Motor pair of poles	Ratio of tachometer freq. to rotor rotational freq.	Selected multiplication factor	Motoring Operation		Braking Operation	
			Desired slip	Adjustment of switch T in Fig. D7	Desired slip	Adjustment of switch Y in Fig. D7
p	z	x	s	y	s	y
1	60	No solution	.01	No solution	-.01	No solution
1	60	8	.0125	79	-.0125	81
2	60	16	.0125	79	-.0125	81
2	120	No solution	.02	No solution	-.02	No solution
2	120	4	.025	39	-.025	41
3	120	2	.025	13	-.025	No solution
3	120	16	.00625	106	-.003125	107

Table D9 Multiplication, x, and division, y, factors knowing numbers of motor pair of poles, p, tachometer factor, z, and slip for motoring and braking operations.